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Field-effect modulation of conductance in VO_2 nanobeam transistors with HfO_2 as the gate dielectric

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We study field-effect transistors realized from VO_2 nanobeams with HfO_2 as the gate dielectric. When heated up from low to high temperatures, VO_2 undergoes an insulator-to-metal transition. We observe a change in conductance (~6%) of our devices induced by gate voltage when the system is in the insulating phase. The response is reversible and hysteretic, and the area of hysteresis loop becomes larger as the rate of gate sweep is slowed down. A phase lag exists between the response of the conductance and the gate voltage. This indicates the existence of a memory of the system and we discuss its possible origins. © *2011 American Institute of Physics*. [doi:10.1063/1.3624896]

VO_2 undergoes an insulator-to-metal transition accompanied by a change in its crystal structure,[1,2] the mechanism of which is still under debate. The transition temperature of a free crystal is 341 K. Its proximity to room temperature has motivated attempts at fabricating Mott field-effect transistors (FETs) to induce the phase transition by applying a gate voltage. Such experiments have so far been conducted on thin films of VO_2.[3–6] Other interesting applications of VO_2 include memory metamaterials[7] and memristors.[8] Recently, it has been realized that single-crystalline VO_2 nanobeams support single or ordered metal-insulator domains in the phase transition.[9,10] This eliminates the random, percolative domain structures occurring in thin films and allows intrinsic transition physics to be probed. In this letter, we report on electrostatic gating measurements on single crystalline VO_2 beams[9,11] using HfO_2 as the gate dielectric. The devices have a hysteretic response and appear to possess a memory persisting over a large timescale (a few minutes). The field effect studies have been done at different temperatures in the insulating and metallic phases of the system.

The VO_2 beams were grown using the vapor transport technique.[9,12] Electrodes were designed by electron beam lithography followed by etching in Ar plasma (for removal of organic residue) and sputtering of Cr/Au to make Ohmic contacts. Figs. 1(a) and 1(b) show the optical microscope and atomic force microscope images of VO_2 devices. The local gate electrode in the middle (Fig. 1(a)) is fabricated by first depositing a 20 nm layer of HfO_2 by atomic layer deposition and then sputtering Cr/Au on top. The typical width of the beams is 0.3-1 μm, and the thickness is 300-600 nm. Fig. 1(c) shows the resistance of a VO_2 beam as a function of temperature (data from device 1). Stress builds up in the system as it is heated, and the system breaks up into alternating insulator and metal domains.[10] The metal domains first appear close to 341 K and on further heating, grow in size and number. The system becomes completely metallic at a much higher temperature. The temperature at which the system turns metallic varies from one device to another (380-400 K) and is dictated by the stress induced due to adhesion to the substrate. (The nanobeams are embedded in a 1.1 μm thick layer of SiO_2 grown on Si wafers.)

Two and four probe gating experiments were done inside an evacuated variable temperature probe station. Both two and four probe resistances of the same devices were measured (at various temperatures in both the insulating and metallic phases) and found to be similar. This indicates that the contact resistance is negligible compared to the intrinsic resistance of VO_2. We have also confirmed that there is no leakage through the gate.[12] Fig. 1(d) shows the effect of gate voltage on the two-probe conductance of a VO_2 device (device 2) at 370 K. The dc gate voltage is swept slowly in a cycle (of duration 20 min) with limiting values of -2.5 and 2.5 V. (The source-drain current used was set at an ac frequency and monitored with a lock-in amplifier.) Arrows indicate the direction of gate voltage sweep. The response of the conductance is hysteretic. Gate sweeps at different rates were conducted on the devices, with the following observation: the hysteresis loop area and maximum change in conductance become larger on making the rate of gate sweep slower. This is surprising and has been confirmed on several devices.

Figure. 2(a) shows two probe conductance (G) as a function of gate voltage (V_g) at 360 K for device 3 at different gate voltage sweep-rates. The cycle which is swept slowly over 27 min has a much larger hysteresis than the one which is swept faster in 10 min. The area of the loop is computed as $\sum G\Delta V_g$ where the summation extends over one cycle of gate voltage. In Fig. 2(b), it is shown how the area of the loop increases with an increase in the cycle time (i.e., slowing down of the gate voltage sweep-rate). Another intriguing aspect is prominently seen in Figs. 1(d) and 2(a). As we increase V_g up from 0 V to higher positive values (see Fig. 1(d)), G increases. At the extreme value of 2.5 V, V_g is reversed backwards. However, G does not start reducing

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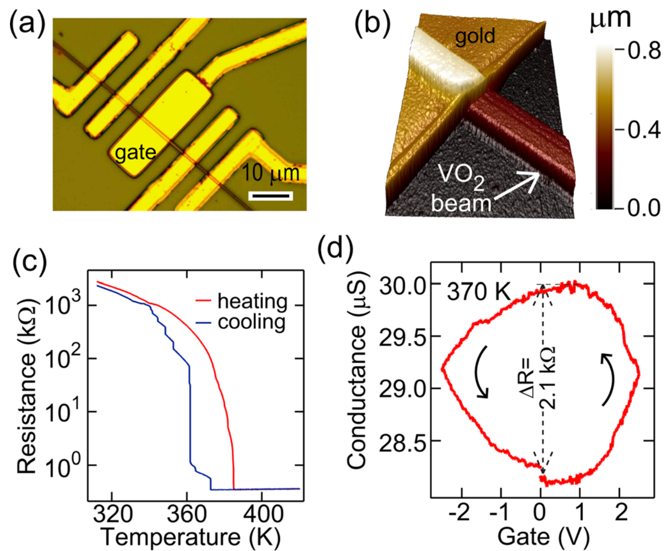

FIG. 1. (Color online) (a) Optical microscope image of a VO_2 device. (b) Atomic force microscope image of a VO_2 device. (c) Resistance (in logscale) as a function of temperature for device 1. The steps in the cooling curve indicate metal-to-insulator transition of individual domains. (d) Conductance of VO_2 as a function of gate voltage (data from device 2). The resistance R, at 0 V to start with, is 35.4 kΩ.

immediately. It goes on increasing for a while and starts to reduce only after a time lag. (Denoting time as t, we can say that $\frac{dG}{dt}$ does not change sign simultaneously with $\frac{dV_g}{dt}$.) This implies that the system wants to persist in the state of "increasing conductance" even though the gate voltage has reversed. This is a manifestation of the "memory" or "inertia" of the system. This memory effect[13] is observed at the other extreme of gate voltage (−2.5 V) also. The gate voltage and resulting conductance (data from device 3) are plotted simultaneously as a function of time in Figs. 2(c)–2(e). (Each plot shows two consecutive cycles of gate voltage.) In all these curves, it is seen that the maximum (minimum) of conductance is shifted in time from the maximum (minimum) of gate voltage. This shift, or "phase lag" between the input and output signals, is the signature of a persistent effect. Slower the rate of sweep, larger is the time-delay. It is 5.6 min for the slowest scan with a 27 min cycle (Fig. 2(e)).

The hysteresis is observed at temperatures at which the beam is in the insulating state or there is a co-existence of metal and insulator domains.[9] No gating is observed in the full metallic state. We compute the "normalized loop area" $\frac{\sum G\Delta V_g}{G_0}$, where G_0 is the conductance at $V_g = 0$. The "normalized loop area" as a function of temperature (close to the metallic transition) for device 3 is plotted in Fig. 3(a). The most prominent hysteresis for our devices is usually obtained in the temperature range 340-370 K, which is the temperature window in which multiple domains exist along the beam.[9,10] Also, it is shown in Fig. 3(b) how the "normalized loop area" varies over a wide range of temperatures (starting from room temperature) for device 1.

Figure. 3(c) shows the gate voltage response (as a time chart) for device 4 at two temperatures. At 370 K, the gate effect (G periodic with V_g) is observed. At 395 K, the VO_2 beam is closer to the full metallic transition and the gate

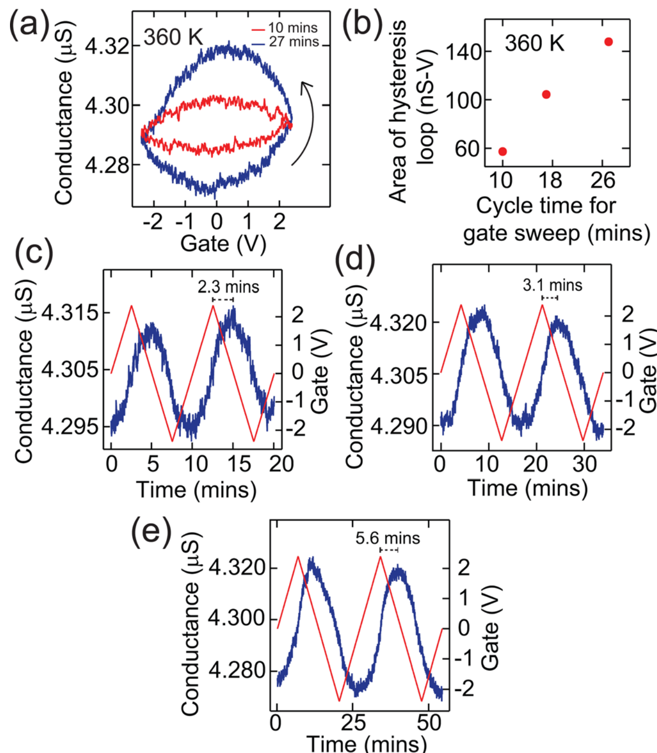

FIG. 2. (Color online) (a) Conductance as a function of gate voltage (device 3) for two different cycle times: 10 min (smaller loop in red) and 27 min (larger loop in blue). (Note: The former (red curve) is offset by −0.009 μS). (b) Area of "conductance vs. gate voltage" hysteresis loop at different cycle times. (c), (d), (e) Gate voltage (triangular pulse in red) and conductance (blue) plotted against time for cycle times 10 min, 17 min, and 27 min respectively.

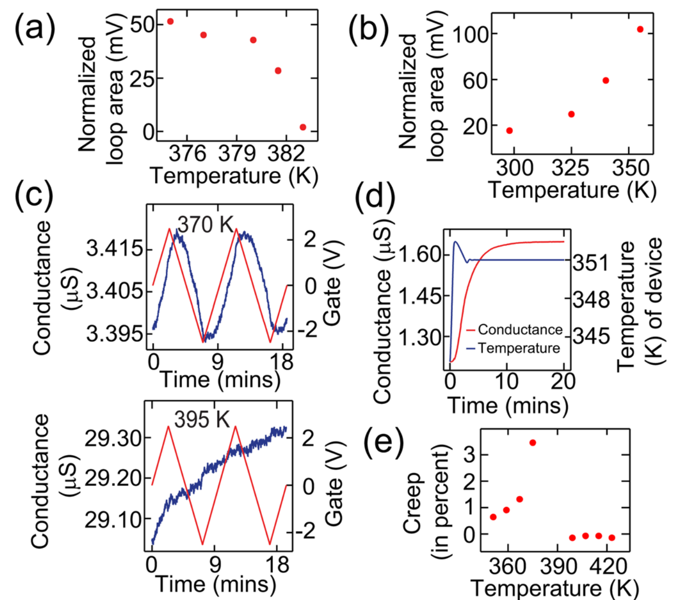

FIG. 3. (Color online) (a) Normalized loop area of "conductance vs. gate voltage" hysteresis close to the insulator-metal transition around 383 K (data from device 3). Cycle time of gate voltage sweep is 25 min. (b) Normalized loop area of "conductance vs. gate voltage" hysteresis at different temperatures in the insulating state of device 1. This was a four probe measurement and time for each gate voltage cycle was 7 min. (c) Gate voltage (triangular pulse in red) and conductance (blue) plotted against time at two different temperatures in the insulating phase of device 4. (Cycle time is 9 min.) (d) Temperature of the sample (device 5) is ramped up rapidly from 343 K to 351 K. The sample temperature reaches 351 K in 5 min, but the conductance keeps on increasing slowly over several minutes after that. (e) Thermal "creep" of device 5 as a function of temperature.

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effect has disappeared. However, there is a gradual variation of the conductance with time. This is the phenomenon of thermal "creep" that we see in our devices. The conductance takes a long time to stabilize after the device is heated to a new temperature. This feature is noticed on all our devices and is illustrated in Fig. 3(d) (device 5). The sample is heated up from 343 K, and it reaches the desired temperature of 351 K within 5 min. However, even 15 min after that, the conductance of VO_2 has not stabilized. It goes on increasing at a slow rate. (The fractional change over the last 10 min is 0.64%.) We define a quantity called "creep" as the fractional change in conductance over a period of 10 min after the sample has reached a new temperature. The variation with temperature of this quantity is plotted in Fig. 3(e). "Creep" becomes quite large just before the metallic transition.

The overall change in G is a few percent ($\sim$6% in Fig. 1(d) and 1% in Fig. 2(e)). Since the entire length of the wire is not covered by the gate, the fractional change in the gated region of device 2 (Fig. 1(d)) turns out to be 14.4%.[12] The gate voltage primarily affects the carrier density close to the surface within the surface skin layer, the bulk being electrostatically screened from the gate. The threshold carrier concentration[14] in VO_2 has been estimated to be 8×10^{18} cm^{-3}. Using this value, it is estimated that the amount of carriers induced by a gate voltage of 2.5 V is 8.3% of the intrinsic concentration. This is close (in terms of order of magnitude) to the fractional change in conductance due to gating. Hysteretic gating effects are known to arise in semiconductors due to the presence of surface states at the dielectric interface. These act as trapping centers for electrons. It has been observed in semiconducting nanowires that on slowing down the rate of gate voltage sweep, the system is allowed time to equilibrate and hysteresis reduces.[15] Hysteresis due to slow traps (with relaxation time of a few minutes) has also been reported.[16,17] But, in the aforementioned cases, the observed behavior on varying the sweep rate is the opposite of what we see in our devices. Hence, trap states do not seem to offer a possible explanation in our experiments.

Persistent effects have been observed in earlier studies on VO_2 (in two terminal memristive devices[8] and infrared response of gated VO_2 films[18]). In our experiments, there is no gate leakage[12] and hence, heating can be ruled out as a possible cause behind the persistent effect. There is not much information in literature about mechanical relaxation in VO_2. It is probable that mechanical relaxation time in VO_2 is quite large. When heated to a new temperature, it would take a considerable period of time for the stress pattern and the relative domain sizes (and hence, conductance) to settle down. This explains the thermal "creep." The VO_2 crystal has electric dipoles with antiferroelectric coupling.[14] The coupling strength will depend upon the spatial separation between the lattice sites, thus providing a coupling between the dipolar arrangement and the strain state. Hence, the gate voltage will also affect the strain state, and relaxation of the dipolar arrangement will have a similar timescale as the mechanical relaxation. This may explain the slow processes leading to the time-delay in gate effects (Figs. 2(c)–2(e)).

In summary, we have fabricated three terminal field effect devices from VO_2 nanobeams using HfO_2 as the dielectric. We observe gate effects in conductance and the response is hysteretic. The dependence of electrostatic gating effects on the sweep rate and a phase lag between the reversal of conductance and gate voltage indicates that our devices have an intrinsic memory with a large timescale of a few minutes. This is interesting from the point of view of probing the physical origin of persistent effect in the insulating phase of VO_2. Also, single crystalline nanobeams with a smaller thickness may exhibit more pronounced electrostatic gating effects and can have important implications in the design of Mott FETs and memory devices.

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Supplemental Material: Field-effect modulation of conductance in VO_2 nanobeam transistors with HfO_2 as the gate dielectric

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Growth of VO_2 beams

The VO_2 nanobeams were synthesized using a modified version of the vapor transport method reported previously.[1] Bulk VO_2 powder was placed in a quartz boat in the center of a horizontal tube furnace. The reaction product was collected on a Si substrate with a thermally grown surface oxide (thickness: 1.1 μm) downstream from the source boat. The growth was carried out at the following condition: temperature 950 C, Ar carrier gas flow rate 10 sccm, pressure $\sim$ 10 torr, evaporation time $\sim$ 4 hours. The size distribution, lattice structure and crystal orientation of these beams were characterized by scanning electron microscopy, transmission electron microscopy and selected area electron diffraction.

Calculation of geometric capacitance

From Fig. 1d of the main text, the maximum fractional change in conductance induced by gate voltage is 6.4 percent. For this particular device (Device 2), the length of overlap between gate and the beam is 7.0 μm, whereas the total length between the source and drain electrodes is 15.7 μm. Therefore, fractional change in conductance of only the region under the gate is 14.4 percent.

We assume that VO_2 and the gate electrode form a parallel plate capacitor, with capacitance C given by $C = \frac{\varepsilon_0 \varepsilon A}{d}$. ($\varepsilon$ is the dielectric constant of HfO_2, A is the area of overlap of the gate with the wire and d is the HfO_2 layer thickness.) The VO_2 beam has a rectangular cross-section, with a width of 400 nm and 230 nm of thickness above the SiO_2 substrate (confirmed by AFM image). The gate electrode is present on three faces, and charges will be induced on the underlying surface. The influence of the electric field will be felt most prominently within the skin depth close to the surface. The breadth of the capacitor is (230+400+230) nm = 860 nm. In our devices, d = 20 nm and considering ε=20, the capacitance is estimated to be 53 fF. The number of carriers induced by a gate voltage of 2.5 V will be 8.3×10^5.

The VO_2 wire is embedded inside the SiO_2 substrate. The total thickness of the wire is taken to be 460 nm (i.e., double the thickness that is 'visible' above the substrate). In an earlier study,[2] the intrinsic carrier density in VO_2 at the insulator-metal transition had been found to be 8×10^{18} cm^{-3}. Using this value, we get the number of intrinsic carriers in

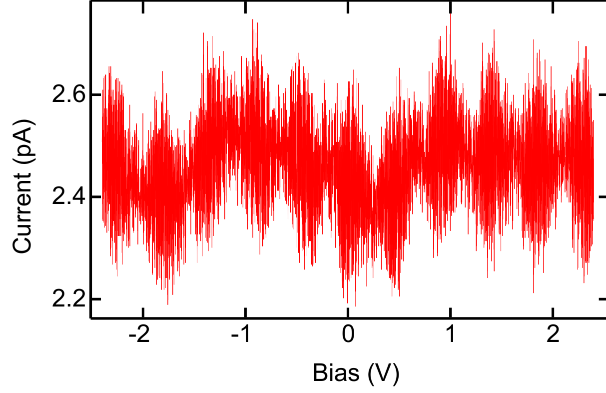

FIG. 1. Current measured between gate and drain electrodes under an applied bias voltage. It is confirmed that there is no leakage through the gate. This measurement was done at 350 K.

the segment underneath the gate electrode as 1.0×10^7. Therefore, the fractional change in number of carriers induced by gate voltage, just by considering a model based on geometric capacitance, should be 8.3 percent.

Measurement of gate leakage

It is crucial in studies of electrostatic gating effects to determine the amount of leakage through the gate. DC current-voltage measurements were done between the gate and drain electrodes of our devices. The magnitude of maximum dc bias was the same as what is used in gating measurements. A typical plot is shown in Fig. 1. The current of approximately 2.5 pA is the noise level of the current preamplifier and there is no change with gate-drain bias voltage. This indicates that there is no current flowing through the gate dielectric. From the given data, we can say that in our devices, there is no leakage of current through the gate which can contribute to the signal being measured.

Measurement of capacitance as a function of gate voltage

Capacitance was measured as a function of a gate voltage both in the insulating and metallic phases of the system. The plots are shown in Fig. 2. The qualitative nature of the plots are similar to the ones reported recently by Yang et. al.[3].

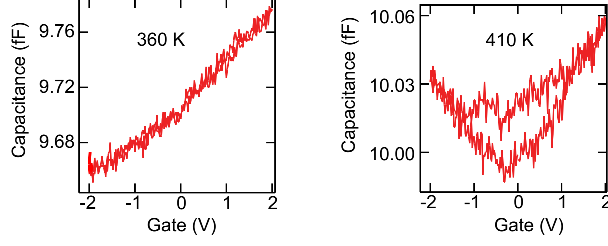

FIG. 2. Capacitance as a function of gate voltage in the insulating (left) and metallic (right) phases.

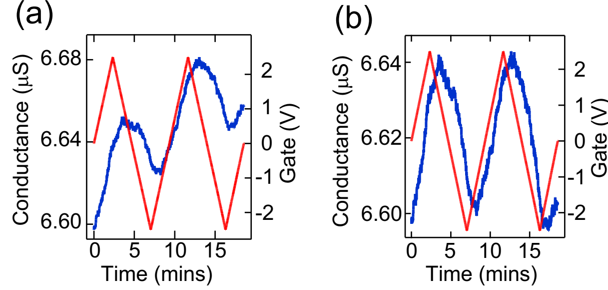

FIG. 3. (a) Conductance and gate voltage plotted simultaneously as a function of time. The periodic behaviour of conductance arises from the gate response, whereas the constant slope is due to thermal 'creep'. (b) Data of the previous figure after subtracting a constant background.

Discussion on thermal 'creep'

We have discussed in the main text about the phenomenon of thermal 'creep'. The conductance of VO_2 takes a long time to stabilize after being heated to a new temperature, even though the temperature of the stage stabilizes quickly. On heating the device to a new temperature, we usually wait for about 30-60 minutes so that the conductance can stabilize before gating measurements are started. If sufficient time is not allowed, then the thermal 'creep' can be noticeable in the measurements.

In Fig. 3a, the conductance and gate voltage are plotted as a time chart. The periodic behaviour results from the applied gate voltage, whereas the overall slope shows that the conductance had not stabilized completely when the scan was started. However, the 'creep' is a slow process, and it can be assumed that over the time when the gate voltage sweeps are conducted, the change in conductance due to 'creep' is proportional to the time elapsed. Therefore, on subtracting a linear background slope from Fig. 3a, we get back the

characteristic change in conductance due to gate voltage only (Fig. 3b).

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