Introduction

Today, there is a great impetus towards producing chips with copper interconnection in microelectronics industry. Copper integration, when combined with low-k materials, promises much faster devices with less complexity and remarkably lowers power consumption. Expected cost of copper processing, however, is lower compared to conventional Al/SiO_2 scheme. Since the introduction of damascene process in 1985 by IBM, there have been several significant developments to meet the requirements for the fabrication of such devices in the near future. Reaching this goal highly depends on developing a viable copper thin film deposition technique.

In this paper, first we will describe general characteristics of damascene process. Then, we will examine the current status of copper thin film deposition techniques developed over the past 15 years. Here, we will especially concentrate on CVD and electrochemical deposition techniques as they give the most favorable results. Finally, we will give an outline for the future trends.

Copper Damascene Process

Copper replaces aluminum as a metallization material due to its high electromigration resistance. This high resistance prevents the copper atoms in interconnection lines from migrating under high current density [Mahajan et al., 1999]. Several other benefits make copper an even more attractive material for metallization. The use of copper interconnection helps reduce RC time delay dramatically. The RC time delay results from two factors: resistance and capacitance. The low resistivity of copper and reduction in length by using vertical interconnections reduce the resistance, while the thinner copper lines cause the capacitance to decrease. Therefore, overall RC time delay drops in copper interconnections. In addition, using copper leads to lower manufacturing costs compared to aluminum and companies that adopt copper early are sure to win favor from stockholders [Singer, 1998].

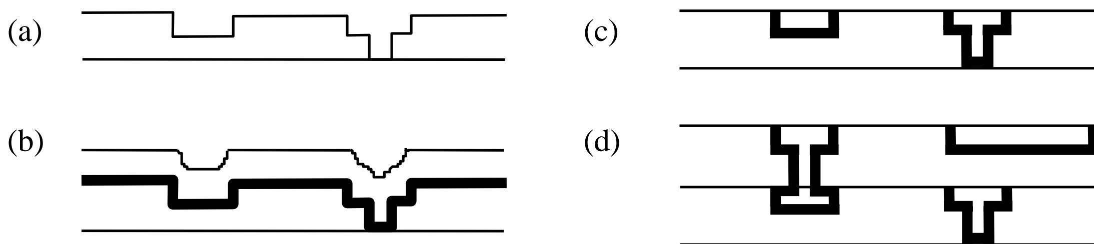


Figure 1. Inlaid metal scheme used to define copper interconnects; (a) trenches and vias are first etched into the ILD; (b) the titanium liner and copper metal are next deposited to fill trenches and vias; (c) the copper is removed above the ILD by CMP leaving the surface planar and the trenches and vias filled with metal; and (d) the sequence is repeated for multiple levels of metal [Steigerwald et al. 1994]

The introduction of copper as a new material for interconnection in integrated circuits prompts the need for a new metallization scheme due to many technical difficulties associated with copper. Copper is known as a fast diffuser and can act to “poison” a device, creating a failure once it gets into the active area (i.e., source/drain/gate region of the transistor). It also exhibits poor adhesion to silicon dioxide and is reactive to the environment [Harper et al., 1994]. Besides, the dry etching of copper has been extremely difficult [Sainio et al, 1996]. The new scheme that can accommodate all the problems is called the damascene process which is illustrated in Figure 1. This process begins with growing a silicon dioxide layer on a silicon substrate, then etch the silicon dioxide dielectric layer into a “damascene” pattern. A film of diffusion barrier material such as Ti, TiN, Ta, etc. is first deposited onto the damascene pattern by CVD because conformality is required here. Copper is then chemically or physically deposited on top of the diffusion barrier layer until the vias and trenches are all filled up.

Finally, the copper surface is polished by CMP process to eliminate excess copper and diffusion barrier, and planarize the surface [Steigerwald et al, 1994].

The copper and silicon diffusion barriers that have been studied can be classified into six groups: (1) polycrytalline transition metal barriers, such as, Ti ,Ta, W, Mo, etc.; (2) polycrystalline or amorphous transition metal alloy barriers, such as, TiW, a-$Ni_{60}Nb_{40}$, a-$Ir_{45}Ta_{55}$, etc.; (3) polycrystalline or amorphous transition metal-silicon (including silicide) barriers, such as, $TiSi_2$, $CoSi_2$, $CrSi_2$, etc.; (4) polycrystalline or amorphous transition metal-nitrogen (including nitride), such as, TiN, $TiN_{0.95}$, $Ti_{45}N_{55}$, etc., -oxygen (including conductive oxide), such as, RuO_2, Mo-O, etc., and -boron (boride) barriers, such as, TiB_2, etc.; (5) amorphous ternary barriers, such, as $TiPN_2$, $Ti_{34}Si_{23}N_{43}$, $Ta_{36}Si_{14}N_{50}$, etc., and (6) amorphous carbon barriers. The ideal diffusion/drift barriers between copper and silicon or silicon dioxide need to be chemically stable, free of defects such as grain boundaries (i.e. amorphous) to prevent grain boundary diffusion up to elevated temperature, and resistant to high solubilities and high diffusivities of copper and silicon as well as high mobility of copper. By following this guideline, we can screen out the best available diffusion barrier material [Wang, 1994].

Copper can be deposited onto the diffusion barrier film by electrodeposition methods (such as electroless and electrolytic), sputtering (PVD), and CVD. Table 1 displays the properties of copper obtained by different deposition methods. Although plating-based deposition can provide high deposition rate and low instrument cost, the wet chemical disposal from the process gives rise to serious environmental impacts and may limit the use of copper in IC fabrication. Copper PVD is a conventional technology with high deposition rate, but poor via-filling and step coverage are the problems. As a consequence, CVD is the most attractive approach for copper-based multilevel interconnects in ULSI chips [Li et al, 1994].

Table 1. Properties of Copper Obtained by Different Deposition Methods [Li et al. 1994]

	CVD	**PVD**	**Electroless**	**Electrolytic**
Resistivity (μΩ-cm)	≥2	1.75-2	~2	~2
Impurities	C, O	Ar	seed layer	--
Deposition Rate (nm/min)	~100	≥100	up to 100	~200
Process Temp. (°C)	~250	room temp.	50-60	room temp.
Step Coverage	good	fair	good	good
Via-filling Capacity	good	poor	fair-poor	fair-poor
Environ-mental impact (waste)	good	good	poor	poor

After depositing copper, the wafer is polished by CMP process to obtain a chemically clean and optically flat surface. The process, as shown in Figure 2, consists of essentially two components: the mechanical grinding and the chemical etching [Murarka et al., 1993]. During the CMP process, the protruded region will be impinged by particles in the slurry, causing dislocation and strain within the surface and even leading to atoms or atom clusters being dislodged from the surface. These dislodged materials or strained surface layers react with chemicals in the slurry at the rates faster than those between chemicals and unstrained layers. This anisotropy in chemical etching and mechanical abrasion produce global planarization of the surface [Luo et al., 1997]. Due to numerous impurities produced in the process, post-CMP cleanup is required to achieve a chemically clean surface. Typically, the process aims to remove foreign particles from the surface by using brush scrubbing, hydrodynamic jets, and ultrasound. Brush srubbing is effective for particles larger than 1 micron, while efficiency of ultrasound lies in the submicrometer range and the hydrodynamic jet method work well in the range between the previous two [Steigerwald et al., 1997].

Figure 2. A schematic cross-sectional view of the polishing tool with wafer under the wafer carrier [Murarka et al., 1993].

Copper CMP is still in the development stage. Many challenges have to be overcome to create a manufacturable copper CMP. The first challenge is that copper is a soft material and prone to surface defects. The second challenge arises from the difficulty in the selection of slurry with proper chemistry and a pad with suitable physical properties [Carpio et al, 1995]. Excessively high pad roughness can cause dishing on the surface, while excessively low pad roughness results in low polish rate. However, if the copper is not fully dissolved, it will redeposit onto the surface in the form of copper or copper oxide particulates. Redeposition of copper reduces the effiency of mechanical abrasion and therefore lowers the polish rate. Redeposition of copper as oxide particulates increases the defect density in the metallization layer [Steigerwald et al, 1995].

Chemical Vapor Deposition (CVD) of Copper

CVD is the most attractive technique for copper deposition due to its ability to involve substrate surface into the deposition reaction. It can produce conformal blanket deposition for void free filling of aggressive via and hole structures at near bulk resistivity and high growth rates. For example, there are experimental studies showing successful CVD deposition of copper on patterned TiN structures with feature sizes as small as 0.3 μm with aspect ratios up to 6:1 [Braeckelmann et al., 1996]. In addition, CVD displays an intrinsic potential for selective copper growth, which may eliminate subsequent etching or polishing. It is relatively simple and controllable, and leads to good adherence, high uniformity over large area. It also reduces susceptibility to interfacial mixing and cross-contamination effects due to relatively low temperatures involved (as low as 150 ^oC) [Kaloyeros et al., 1993].

In copper CVD method, a copper source (precursor) is delivered to a heated substrate where, upon contact, it decomposes into metallic copper and gaseous byproducts that are pumped away. Inorganic precursors such as copper halides proved to be extremely problematic due to their low volatility. When the temperature is raised over 400 ^oC, they lead to production of corrosive byproducts such as hydrochloric acid and hydrofluoric acids and produce large concentrations of halide contaminants [Bouhila et al., 1997]. Among the metal-organic copper precursors, copper (II) and Lewis base-stabilized copper (I) β-diketonate compounds, whose chemical structures are shown in Figure 3, have attracted most of the research efforts due primarily to their relatively high volatility. Table 2 summarizes the main properties of representative members of each group.

Cu (II) precursors have several disadvantages such as frequent introduction of impurities, requirement of reducing agents and fairly high temperatures. As Cu (I) precursors have recently received much more attention, the rest of the discussion in this paper will concentrate on them. These compounds deposit pure copper films via a quantitative bimolecular disproportionation reaction on the surface where two Cu(I) species react to form a Cu(II) compound and a copper atom in the absence of

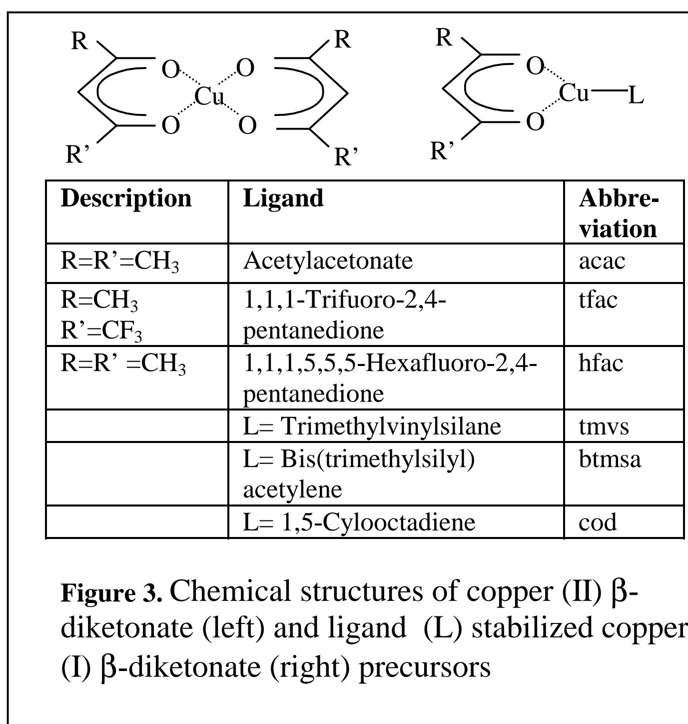
reducing gas or carrier gas. For the precursor $(hfac)Cu^{I}(tmvs)$, this disproportionation reaction can be written as

$$2(hfac)Cu^{I}(tmvs) \rightarrow Cu^{0}(s) + Cu^{II}(hfac)_2(g) + 2(tmvs)(g) \quad (1)$$

According to the generally accepted model, the first step is the chemisorption of the precursor onto the substrate surface and its dissociation into the (hfac)Cu and (tmvs) species. (Tmvs) is highly volatile and quickly desorbed leaving $(hfac)Cu^{I}$ species behind. During the last step of the reaction, two $(hfac)Cu^{I}$ species react to form copper metal and $Cu^{(II)}(hfac)_2$ which is volatile and easily desorbed from the substrate surface [Doppelt et al., 1994]. In a recent study, Chae et al. observed negligible decomposition of $(hfac)Cu^{I}(tmvs)$ precursor on the active surface sites. Instead, it decomposed into (hfac)Cu and (tmvs) via gas phase reactions, and (hfac)Cu was the real precursor. Gas-phase reactions preferentially formed (hfac)Cu instead of (tmvs)Cu because the bonding energy of Cu-tmvs is weaker than that of Cu-hfac. Their conclusion was that the surface reactivity of (hfac)Cu governed the growth rate of Cu film at low temperatures. At higher temperatures, the gas phase reactions that produce this intermediate species are rate limiting [Chae et al., 1998].

Table 2. Properties of Representative Copper Precursors from the Two groups [Gelatos et al., 1994]

$Cu^{II}(hfac)_2$	$(hfac)Cu^{I}(tmvs)$
Solid	Liquid
Decomposition at T> 200 °C	Decomposition at T> 40 °C
Vapor pressure ~10 Torr at 100 °C	Vapor pressure ~0.3 Torr at 40°C
Reducing agent required for pure films	Disproportionation reaction
Insufficient conversion to copper	Efficient conversion to copper



Description	Ligand	Abbre-viation
R=R'=CH_3	Acetylacetonate	acac
R=CH_3 R'=CF_3	1,1,1-Trifuoro-2,4-pentanedione	tfac
R=R' =CH_3	1,1,1,5,5,5-Hexafluoro-2,4-pentanedione	hfac
	L= Trimethylvinylsilane	tmvs
	L= Bis(trimethylsilyl) acetylene	btmsa
	L= 1,5-Cylooctadiene	cod

Figure 3. Chemical structures of copper (II) β-diketonate (left) and ligand (L) stabilized copper (I) β-diketonate (right) precursors

Using $(hfac)Cu^{I}(tmvs)$ as the precursor (the commercially available form is called CupraSelect®), several researchers identified two distinguished temperature regimes in the Arrhenius plot of the growth rate vs. 1/ T_s (substrate temperature): a surface-reaction-controlled regime at lower temperatures and a transport-limited regime at higher temperatures [Bollmann et al., 1997 and Marcadal et al. 1999]. However, increasing the temperature of bubbler (T_b) has no effect on the deposition rate. For a given T_b, a higher T_s leads to the formation of larger copper islands in a smaller number density. Conversely, at a given T_s, a higher T_b (equivalently at a higher precursor feed rate) results in the formation of smaller islands in a higher number density. This trend can be understood based on the nucleation theory which predicts that heterogeneous nucleation rate increases with decreasing T_s and increasing deposition rate to favor smaller nuclei to be formed in a higher density. Experimental results seem to indicate that the nucleation rate is enhanced at higher T_b

even in the surface-reaction-controlled regime where the deposition rate depends only slightly on T_b [Hwang et al., 1998].

Increasing the temperature, to achieve higher deposition rates, introduces contaminants (mainly carbon) to film and increases the resistivity [Cho et al., 1997]. This is primarily due to decomposition of the volatile by-products at elevated temperatures (over ~250 ^oC). In addition, uniformity of deposition becomes considerably worse with increasing temperature due to feed rate limitations. Decreasing the precursor flow has the same effect [Wolf et al., 1999]. Addition of water vapor has been suggested to enhance deposition rates. The deposition rate increases significantly without degrading the copper resistivity with the optimum concentration at P_{water} = 0.2 Torr. The higher deposition rate with water is believed to arise from an increased conversion efficiency of the precursor to copper film. In addition, the presence of water vapor produces denser films with lower incubation time [Gelatos et al., 1994]. In general, the CVD copper films have a FCC structure with (111) preferred orientation at all substrate temperatures. Impurity levels in copper films at careful experimental conditions are under the detection limits of AES. The increased resistivity of CVD films is mainly caused by grain boundaries [Riedel et al.,1997].

Many researchers have observed higher levels of copper deposition on metals relative to oxides during copper CVD with both copper (I) and (II) type precursors. Most common explanation for the observed selectivity when copper (I) type precursors are used is the following. The bimolecular disproportionation reaction involved in precursor decomposition requires electron transfer between the metal centers and can therefore be catalyzed by conducting (metallic) but not insulating (oxide) surfaces [Kim et al., 1998]. This opened up an avenue to develop selective copper CVD deposition in which, growth occurs only over the desired areas of a patterned substrate surface. However, an inherent danger is the loss of selectivity before the end of the deposition step. Several publications have shown that, the presence of hydroxyls on the insulator surface can result in the loss of selectivity [Dubois et al., 1992]. Attempts to eliminate hydroxyls include the anneal of SiO_2 to temperatures of about 800 ^oC prior to deposition of copper [Gelatos et al., 1994], chemical passivation of hydroxyls by introduction of methyltrichlorosilane [Jainet et al.,1993] and hexamethyldisilane (HMDS) [Doppelt 1997]. A recent study indicated that the extent of passivation also depended on type of the carrier gas. If H_2 is used as the carrier gas, passivation with HMDS is not efficient whereas HMDS with Ar as the carrier gas gives promising results [Kim et al. 1998].

For copper applications both types of conventional CVD reactors (hot-wall or cold-wall) have been examined. As hot-wall reactors are heated chambers, interior of the furnace also becomes coated with copper, resulting both in maintenance problems and reduced efficiency. On the other hand, cold-wall involve heating the substrate alone, either inductively of resistively. Despite their complexity, these reactors allow greater control over process parameters. Nowadays, PECVD and PACVD, in which energy imparted to the reactant gases to excite the precursor molecules either directly or indirectly through the carrier gas, are gaining interest for copper deposition. RF and microwave induction are generally used for plasma generation. PACVD employs much lower plasma densities than PECVD to avoid plasma-induced physical damage in the substrate and undesirable changes in its electrical characteristics. In the case of copper (I) compounds, plasma could also be applied to help dissociation of copper (I) parent molecule into the copper (II) molecule, leading to a more efficient conversion to copper, and thus increased growth rates. Since (hfac)Cu^I(tmvs) is liquid, it can be transferred to reactor with a conventional bubbler-based delivery system. Recent study of Braeckelmann et al. showed that the more efficient approach is to use the newly-developed direct liquid injection (DLI) system for precursor delivery. It allows precise control of precursor flow within a wide delivery window (0.01-5.00 cc/min). In their study, base pressure was $2x10^{-6}$ Torr (typical range in copper CVD 10^{-7} to 10^{-5} Torr) while pumping speed was 220 l/s [Braeckelmann et al., 1996].

Other deposition methods for copper damascene

Physical vapor deposition (PVD) and eletrodepostion are other possible deposition techniques for copper damascene process. Copper PVD has been considered unsuitable for copper damascene process due to its poor conformality and self-shadowing (creation of voids) effects in depositing high aspect ratio features [Wenzel et al., 1997]. This shortcoming arises from the fact that the sputtered efflux coming off the surface of the sputter target is a cosine distribution. This wide angular distribution of metal vapor produces overhang features and ultimately void formation when filling vias and holes. However, recent studies showed that ionized physical vapor deposition (IPVD) could solve this problem by ionizing the metal vapor efflux from the sputter source using a second discharge [Foster et al.,1998 and Grapperhaus et al., 1998]. The angular distribution of the metal ions can then be controlled by biasing the substrate. The electric field associated with the sheath at the substrate collimates the ion flux forming a beam of ions normal to the substrate and thereby achieving fills of high aspect ratio features with little overhang or void formation. A schematic of a typical IPVD apparatus is shown below:

Electrodeposition, which includes electroplating and electroless deposition, holds the advantages of low tool cost, low processing temperature and the ability to achieve high selectivity, good step/trench filling and excellent step coverage [Shacham-Diamand et al., 1997]. In the case of electroplating of copper, the wafer is typically coated with a thin conductive layer of copper (seed layer) and immersed into a plating solution containing cupric ions. Electric contact is made to the seed layer, and current is passed such that the reaction $Cu^{2+} + 2e \rightarrow Cu$ occurs at the wafer surface [Andricacos et al., 1998].The principle of electroless deposition is very similar to that of the electroplating process except that it does not require power supply, the electrons needed for the metal reduction are supplied by the simultaneous oxidation of a reducing agent in the solution. Since the underlying mechanism for these two processes are very similar and the electroless deposition is more complicated than electroplating, the former method will be selected as an example for detailed discussion.

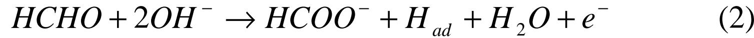
Table 3. Typical bath composition for electroless copper deposition [Shacham-Diamand et al., 1997]

Chemicals or other parameters	**Range**
CuSO4 5H2O	0.016-0.08M
Formaldehyde	0.13-1M
EDTA	0.03-0.27M
Polyethylene glycol	50-100ppm
2-2'-Dipyidyl	10-120ppm
CN-	0.01-0.1M
pH adjustment with TMAH	11.4-13
Temperature	30-80 °C
Surfactant	N/A

Figure 4. Pictorial representation of the experimental apparatus used for the ionized physical vapor deposition studies [Reid et al., 1998]

Electroless deposition has a very complex reaction chemistry which involves many chemicals, a typical bath composition and the concentration range of these chemicals are given in Table 2. (Here, EDTA: Eethylenediaminetetraacetic acid; TMAH: Tetramethylammonium hydroxide; TEAC: Tetetraethylammonium cyanide; HCHO: Formaldehyde).

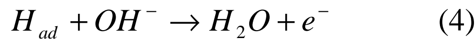
EDTA is used as a strong complexing agent keeping cupric ion soluble in high pH, surfactant works as the wetting agents in order for the hydrogen gas bubble easy to detach from the deposited film. The solution pH is maintained by TMAH rather than sodium (potassium) hydroxide because the latter can introduce alkali metal ions that contaminate the copper film. Formaldehyde is the most commonly used reductant in this process. The overall reaction can be written as [Mak et al., 1994]:



$$HCHO + 2OH^- \rightarrow HCOO^- + H_{ad} + H_2O + e^- \qquad (2)$$

This reaction has a positive potential, thus is thermodynamically favorable. The hydrogen adatom product can either undergo surface diffusion and recombine to form hydrogen gas, as indicated by reaction (3) or can be further oxidized to water (reaction (4))

$$2H_{ad} \rightarrow H_2 \qquad (3)$$



$$H_{ad} + OH^- \rightarrow H_2O + e^- \qquad (4)$$

Reaction (3) should be avoided because evolved hydrogen can be trapped inside the film and form voids, which will lower the Cu ductility. It is experimentally observed that Reaction (3) is much easier to happen on Cu, Au, and Ag substrates than Pt and Pd. This can be explained by the fact that the exchange current density of hydrogen reduction on Cu, Au and Ag is very small ($<10^{-6}$ A/cm), while it is several orders of magnitude larger on Pt or Pd ($>10^{-4}$A/cm). So the hydrogen reduction reaction (4) is very easy to occur on Pt or Pd, while it very difficult on Cu, Au and Ag [Mak, et al., 1994].

Under normal conditions, it was observed that reaction (2) did not happen even though it is thermodynamically favorable. This is due to the high activation energy associated with this reaction which limits the copper deposition rate. Some catalysts can decrease the activation energy and dramatically increase the deposition rate. In terms of electroless deposition, some conducting materials that are capable of transferring electrons could remarkably accelerate the reaction rate. For this purpose, Cu is considered to be the most effective catalyst than any other metals. However, it is often very difficult to start the first layer of Cu. This technical difficulty can be circumvented by first depositing a very thin seed layer (e.g. Au, Pt and Pd) on the substrate. Once the first Cu layer is formed, the reaction rate will be greatly increased and this autocatalystic effect will continue until all the reactants are used up[Cho et al., 1993].

Generally, the microstructure of electroless deposition follows the crystallographic characteristics of the substrate [Mak, C.Y. et al.]. Epitaxial growth is inherent with electroless copper deposition. This should not be surprising in terms of the high mobility of copper atoms and the fact that copper can recrystallize easily. Furthermore, since copper is a good conductor as well as a perfect catalyst for fomaldehyde oxidation, nucleation is expected to be uniform on all growth fronts, favoring epitaxial growth. The imperfection of the deposited copper film is mainly caused by the entrapped hydrogen gas inside the material, which results in many voids and increases the film internal pressure. Even though low temperature (<150°C) annealing could liberate the trapped the hydrogen and eliminate the pressure effects, the internal voids are very difficult to remove[Cho et al., 1993].

One major concern arising from the electrodeposition process is copper contamination of the wafer bevel and backside. The most effective method to eliminate this source of contamination is to ensure that the bevel and backside of the wafer do not come in contact with the bath. Combining this method with a post-plating rinse can effectively eliminate copper contamination issues associated with this method. Another concern of electrodeposition is most semiconductor process engineers have little experience with this approach, which leads to a preference for more familiar copper-fill methods, like CVD or directional PVD combined with reflow. But the low-cost of electrodeposition provides a strong motivation for process engineers to examine it thoroughly. Once manufacturing-worthy electrodeposition equipment becomes widely available, copper electrodeposition technology should gain much acceptance [Jackson et al., 1999].

Conclusion and Future trends

As a new technology, copper damascene process has been greatly improved in the past years. There exist several publications indicating that both CVD and electrochemical plating techniques are becoming established methods for copper deposition. Studies on copper CVD have not only resulted in a better understanding on the fundamental phenomena but also opened a window for selective copper deposition. Selective deposition process demonstrates a great promise for simplification of copper integration by elimination of subsequent CMP or other planarization processes[Cho et al.,1993]. Despite its recent introduction just a few years ago, electrochemical plating is proved to be a comparable deposition technique over to electroless deposition. Indeed, recent trends showed that it might be the preferred deposition technique in the future.

Achieving smaller and smaller feature sizes have been an everlasting trend in the microelectronic device fabrication and it will continue to be so. As reported by Daily California, microscopic copper wires will soon be making microchips that are nanometers wide or even thinner, thanks to findings of a Lawrence Berkeley National Laboratory scientists. Othon Monteiro devised a new method to create even smaller microchips by using “iron-assisted trench filling” to form fine copper wires on wafers, unlike standard methods that cause trenches to fracture more readily [Lee, 1999].

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