

INTERCONNECT OF NEW MILLENNIUM: COPPER

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FALL 1999

Abstract

A new era in chip manufacturing is about to start with use of copper as the interconnect metal. Copper, which has been regarded as one of the “poisons” in the microelectronics industry, now makes its way to the “veins” of the integrated circuits (ICs). In this term paper I intend to examine why we need copper this badly and what are the key factors in the transformation from aluminum to copper. I discuss the processing issues pertaining to copper patterning after giving a thorough comparison of aluminum versus copper interconnection.

Introduction and Overview

Modern ICs contain tens to hundreds of millions of logic devices to achieve complex functions. Interconnects which are embedded in interlayer dielectric material (ILD) are the wire connections to supply electrical signals to these devices. In the past thirty years, interconnects have evolved from a single layer of Al to multiple levels of sandwiched Ti/Al-Cu/TiN metal layers in ILD SiO_2 (See Figure 1) [1,2]. Today, the demand for faster and more reliable chips with larger scale of integration is bigger than ever. The major reasons for introducing the copper as the new interconnect metal into the next generation ICs stem from the well-established trends in the IC manufacturing. In essence, the goal is to produce ICs with larger scale of integration, higher device density, lower power consumption and faster clock times. There is also an enormous impetus to reduce the process complexity and cost. However, all of these should be achieved without compromising from the reliability. Increased chip size inevitably translates into longer global interconnect wires. At the 100 nm technology node, which will be introduced for volume manufacturing in the year 2005, ICs are planned to be 5 cm^2 in size with 8 levels of interconnects and the total wire length of about 5 kilometers. These chips will operate at 2 GHz with power supply voltage of 1.2 V or less [3].

Achieving these ambitious goals necessitates substantial changes in the interconnection technology. Because the interconnect delays become a higher percentage of the total delay time at each new technology node, new materials for both ILD and interconnection should be developed to improve delay times. The interconnect material needs to be a better conductor than Al alloys while we need an ILD with lower dielectric constant than SiO_2 (commonly referred as low-k materials). Since main reliability problem with current Al interconnection is the electromigration at higher current densities, new interconnect material should also have superior electromigration resistance. At present, semiconductor industry regards copper as the interconnect material of the new millennium while search for the low-k ILD is still continuing.

Copper satisfies all of the needed requirements for the new interconnect metal. However it diffuses quickly as an interstitial atom in the silicon and several deep levels are well known. Since its introduction by IBM in 1985, a major research effort has gone into making the copper a viable candidate for interconnection [4]. New technologies such as

chemical mechanical polishing (CMP) and electroplating of copper have been developed for copper patterning. This term paper is planned to give a condensed summary of the current copper interconnection technology. The first part of the paper is reserved for the delineation of the motivation for the copper interconnection. Then the second part will give an overview of the copper patterning technology. Later in this section some of the important process steps will be discussed.

Motivation for Copper Interconnection

Copper has several properties that make it very attractive for interconnection. First, copper has a lower resistance compared to aluminum (resistivity for Cu: 1.67, for Al: 2.66 and for Al-alloys: $\sim 3.5 \mu\Omega\text{-cm}$) [5]. Figure 2 shows the effective resistivity of copper and aluminum interconnections at different line widths [6]. This lower resistance is critically important in high performance ICs, because it enables signals to move faster by decreasing the so-called RC time delay. RC time delay is defined as the time it takes for the voltage to reach 63% of its initial value at one end to a metal line when a step input is presented at the other end of the line. The RC time delay is equal to the product of the total resistance and the capacitance of the line [5]. Scaling of the ICs over the years reduced the delay times to a level where major contribution to the total delay today is not due to gate delay but is because of the RC delay. As can be seen from the Figure 3, the role of RC delay would be more significant in the total delay time in next technology nodes [7].

Copper enables a decrease in not only the resistance part of the RC delay, but also it can reduce the capacitance part. This reduction stems from the fact that the metal lines can be made thinner using copper. Using thinner copper interconnect lines in a low-k matrix, one can build ICs which would consume substantially lower amounts of power due to decrease in the total RC (resistance \times capacitance) [8]. Copper lines can be made thinner as copper has superior resistance to electromigration. Electromigration (EM) is defined atomic diffusion in an electric field created by high current densities. EM damage results from occurrence of electromigration flux divergences at grain boundary triple points [9]. It can significantly reduce the reliability of the IC as it can be manifested as hillocks on film surfaces, bridges between two conductor lines or discontinuity in a conductor line as shown in Figure 4 [10]. In silicon technology involving Al interconnects, EM resistance can be increased by using so-called bamboo structure (reduces the possibility of grain boundary triple points) and alloying (addition of 1 to 4% Cu to Al) [11]. However, even with these enhancements, Al-alloys are not able to answer the reliability concerns as the current densities in the interconnects increase with scaling of ICs (more than 10^6 A/cm^2). Metals with higher melting points are less prone to EM as the activation energies for grain boundary diffusion scale well with the melting point of a metal. Copper has a higher melting point (1083°C) than aluminum (660°C), which leads to greater EM resistance. The reports of EM lifetime testing of Cu interconnect show between one and two orders-of-magnitude greater lifetime for Cu as compared to Al-alloys [12]. In essence, high electromigration resistance of copper means that it can reliably handle higher current densities with thinner lines reducing power consumption.

In reality, the most important benefit with copper interconnection beyond the ability to increase chip speed and reliability and reduce the power consumption is that it can actually lead to lower manufacturing costs compared to aluminum.

There are two reasons for the reduction in the costs. The first one is directly related to achieving the tighter packing densities with copper, which is a natural result of using smaller lines. Since higher packing densities can be achieved per level, fewer levels of metallization is needed, resulting in significantly lowered manufacturing costs (see Figure 5). The decline in the number of metallization results in decrease in complexity. The second reason in the cost reduction is due to the advantages brought by the damascene architecture, which is the new process to form the copper interconnect lines. Damascene process requires 20-30% fewer steps than traditional subtractive patterning [8]. Especially use of dual damascene (in which both the via and the interconnect are formed at the same time) eliminates the involvement some of most difficult steps such as aluminum etch, and many tungsten and dielectric CMP steps. Figure 6 compares the subtractive aluminum interconnect fabrication process with the copper damascene process [13]. In summary, copper patterning offers substantial advantages in areas such as speed, power, complexity and cost. Figure 7 summarizes the advantages gained by using copper as the interconnect and a low-k dielectric material as the ILD [14].

Copper Patterning Technology

Patterning Cu using reactive ion etching (RIE) has proved to be difficult due to the fact that volatile copper compounds do not form at the temperatures normally used for RIE (less than 100 °C) [15]. Copper etch processes necessitates temperatures in excess of 250 °C, which leads to significant manufacturing problems such as the stability of etch mask [16]. Therefore, traditional subtractive patterning method, which have been used for aluminum is not appropriate for copper interconnection. The process flow for copper patterning is well established today. Tungsten plugs are used at first level of metal to contact the source, the drain and gate regions, due to concerns over copper poisoning. After these, the rest of the interconnection including the vias is made of copper using single or dual-damascene structures. Figure 8 shows the fabrication steps for a dual-damascene process [13]. Here, the first step is the deposition of a thin layer of SiN, which acts as a barrier against diffusion of copper between metal levels. This layer also serves as an etch stop in the ILD etch process that defines the damascene via. Deposition of ILD (in this case SiO₂) follows the SiN deposition. PECVD is the commonly used method in the deposition of both SiN and SiO₂ layers. After lithograph and via/trench etch steps, a conductive barrier layer is deposited. This barrier layer has two purposes. First one is to prevent copper from diffusing into the ILD SiO₂. The second is to enhance adhesion of copper. Now the wafer is ready for copper deposition. Copper fill can be done by either CVD or electroplating. The trend in the industry is towards using the electroplating as the main deposition technique for copper damascene. Copper deposition is followed by CMP. Copper CMP is used to remove excess copper and planarize the surface. Finally SiN cap layer is deposited. At this point the wafer is ready to next metallization step. In the following sub-sections, some of these steps will be discussed in more detailed.

Diffusion Barrier Layers: Since Cu is a fast diffuser in Si and SiO₂, one should isolate copper metallization from the rest of the IC. Otherwise, Cu impurities degrade the device performance by introducing deep electronic levels into the Si band gap resulting in the reduction in minority carrier lifetime. Furthermore, the presence of Cu-Si precipitates in critical regions intensely affects the reverse leaking current of p-n junctions. The maximum surface concentration on Si is required to

be below 2.5×10^9 atoms/cm² with the reducing geometric dimensions [17, 18]. Hence, effective diffusion barriers are the key elements of the copper interconnection. Two types of diffusion barriers are required; first one is the dielectric barrier (commonly SiN) and the second one is conductive barrier (commonly Ta or Ta-based alloys). Because even very thin layers are effective in preventing copper migration, SiN is an attractive material as the dielectric barrier [19]. Usually high-density plasma methods rather than traditional PECVD methods are used in deposition of SiN to obtain dense and pinhole free thin films with low stress. In the field of conductive barriers, several refractory metals and their compounds have been fundamentally studied including TaSi_x, TaSi_xN_y and TaSi_xO_yN_x as well as Ti/TiN and TiW [17,18,20]. As the line widths diminish, the barrier layer causes a significant increase in the line resistance. Therefore, the barrier layer should be very thin and concurrently stable enough to provide reasonable barrier properties. Currently, most satisfactory conductive diffusion barriers are Ta-based alloys. Research activities are concentrated on developing viable LPCVD for Ta-based conductive diffusion barriers, particularly because its ability to provide good step coverage and possible selectivity [20].

Copper Deposition: Until recently CVD was the most accepted method for copper deposition. However, electroplating of copper became the preferred method for copper fill in the damascene patterning with the recent developments in this area [8, 21]. Electroplating offers a very inexpensive and simple process with good step coverage and void-free filling at high deposition rates. When the electrolyte composition is well adjusted, electroplating inside trenches starts preferentially on the bottom. Organic additives to the copper plating solution improve the fill properties by repressing the deposition rate. Interior regions of trenches are less accessible by these additives, so less suppression occurs there, causing higher deposition rates. This unique aspect of electroplating is called super filling. This way high-aspect ratio trenches can be filled successfully (See Figure 9)[13].

In addition to void-free filling, more reliable interconnects can be made by electroplating as it is easy to manipulate microstructure by using organic additives. According to a recent study the deep sub-micron CVD Cu interconnects possess fine grain structure while it is straightforward to get larger grains with near bamboo structure by electroplating. Consequently, the electroplated Cu interconnects have been shown to resist EM damage much better (See Figure 10) [22]. A potential drawback of electroplating is that it is a two-step process. CVD can complete the copper fill in one step directly on the top of the diffusion barrier layer. However electroplating necessitates deposition of a thin seed layer prior to the plating fill step (by CVD or PVD). The seed layer supplies a low-resistance conductor for the plating current that drives the electrodeposition process. It also assists the nucleation of the plated copper film. Even though electroplating is a two-step process and increases the number of process steps, because of its super filling and better microstructure characteristics it is accepted as the mainstream deposition technique for copper patterning.

Chemical Mechanical Polishing (CMP): CMP involves both chemical and mechanical processes to remove the excess copper and achieve global planarization on the wafer surface. Figure 11 illustrates the general features of CMP process. Here, chemically active slurry, which contains of sub-micron size particles, is utilized to polish and planarize the wafer. Rotational speed and the pressure directly determine the extent of polish rate [16,23,24]. Copper CMP involves two

concurrent processes: mechanical abrasion of the surface followed by chemical dissolution of the abraded material in the slurry. The chemistry of the slurry should be adjusted such that it would electrochemically dissolve the abraded material (copper, copper oxides, copper hydroxides etc.) but keep the dissolution from the surface of the wafer minimal. The surface dissolution should be as low as possible to minimize isotropic etching, which would decrease the planarization efficiency. If the slurry is chemically too active it would also cause dishing problems. Dishing is defined as excessive removal of material in large surface area trenches relative to lower surface area lines and vias [15]. Slurries, which contain complexing agents such as ammonia [23, 25] or glycine [26,27] are most promising for copper CMP. These slurries allow lower surface etching but dissolve the abraded particles and chemically stabilize the copper ions through chelating action. The post-CMP clean step is crucial to remove any copper remaining on the bevel or the backside of the wafer.

Conclusions and Closing Remarks

Integration of copper into ICs as the new interconnect metal has been discussed. Since it is hardly possible to cover this huge topic in detail with the present size restrictions, the author intended to give a condensed summary. It is apparent that benefits gained by use of copper patterning are so extensive that microelectronics industry is willing to pay the price for the development of completely new technologies. In the past ten years we have witnessed an enormous effort to build up a bottle-neck-free copper interconnection technology. Today we have highly improved conductive barrier layers made of Ta-alloys that allow us to keep the copper away from devices. Recently, the electroplating technology has become the mainstream method for cheaper, simpler void-free copper fill. Of course there still are many problems to be solved. Fundamental mechanisms governing copper CMP have not been fully understood. This explains why there is no commercial slurry for copper CMP yet. Copper CMP, which is a complex process by its nature, should be turned into a mature technology by concentrated research efforts. The contamination issues with copper will be always a concern. Therefore research on the better barrier layer and post-CMP cleaning will likely to increasingly continue. Copper is only the one of the two legs for walking towards faster chips. Suitable low-k materials for ILD should also be developed. Patterning of copper in these new materials would define the new line of research efforts at the beginning of the millennium.

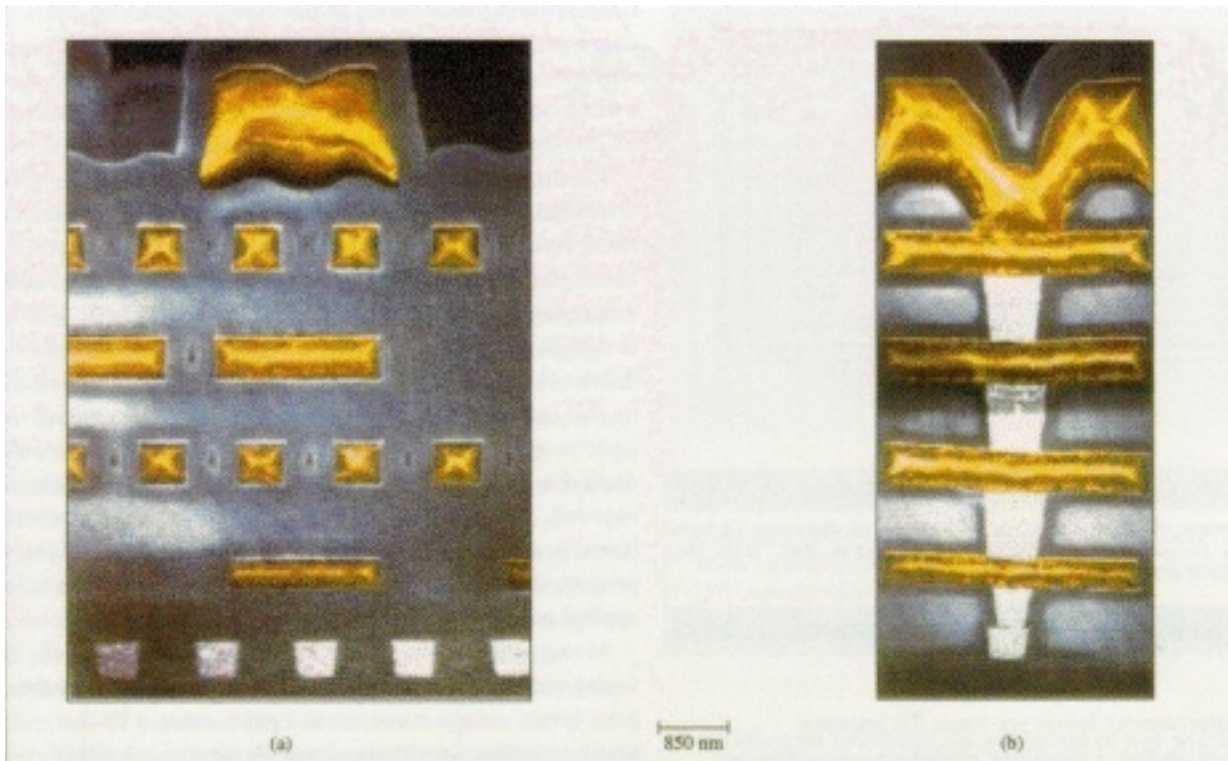


Figure 1. SEM pictures from different parts of the wafer showing the interconnect structures made of multiple levels of sandwiched Ti/Al-Cu/TiN metal layers in ILD SiO₂. (a) One local and five global interconnect levels (b) stacked contacts and vias. The micrographs are artificially colored for better contrast. (From reference 1).

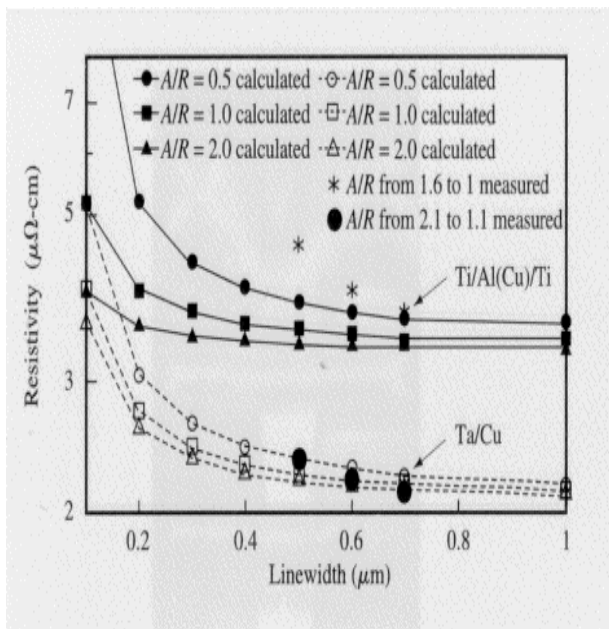


Figure 2. Comparison of effective resistivity versus line widths of trenches for copper and Al-Cu alloy interconnection (from reference 5)

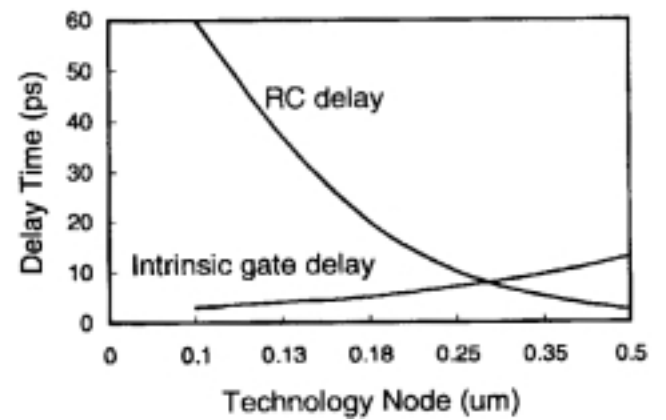
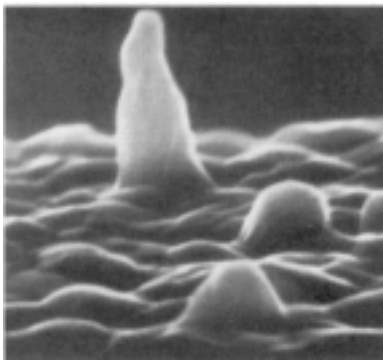
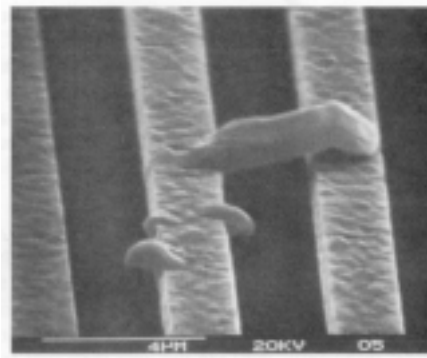


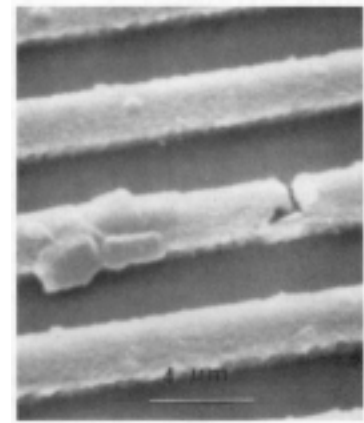
Figure 3. Intrinsic gate delay and interconnect RC delay at minimum design rules of each node (From reference 5).



(a)



(b)



(c)

Figure 4. Manifestation of electromigration damage in aluminum films (a) Hillock formation, (b) whisker bridging between two conductor lines, (c) mass accumulation and depletion (From reference 10)

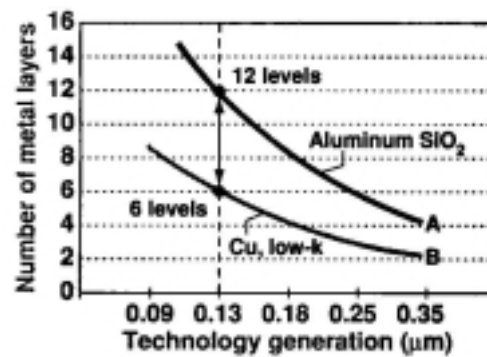


Figure 5. One of the main benefits of copper beyond the ability to increase chip speed and reduce power consumption is that the number of metal levels can potentially reduce as much as half (from reference 8).

DAMASCENE Technology Roadmap

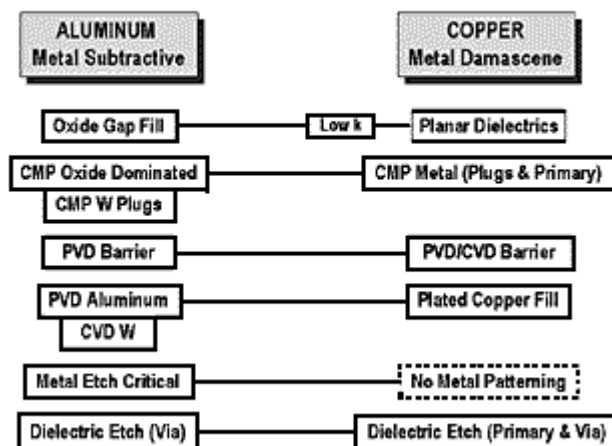


Figure 6. Summary of the major process technology changes required in the transition from the subtractive aluminum interconnect fabrication process to the copper damascene fabrication process (from reference 13).

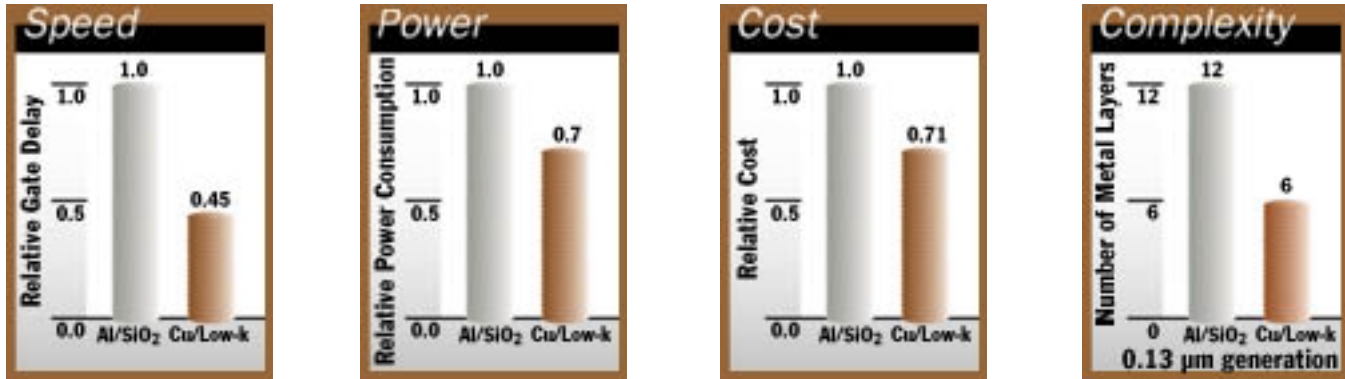


Figure 7. Comparison of copper interconnection with low-k ILD material versus traditional aluminum interconnection with SiO₂ (from reference 14).

Dual-damascene Copper Process Sequence

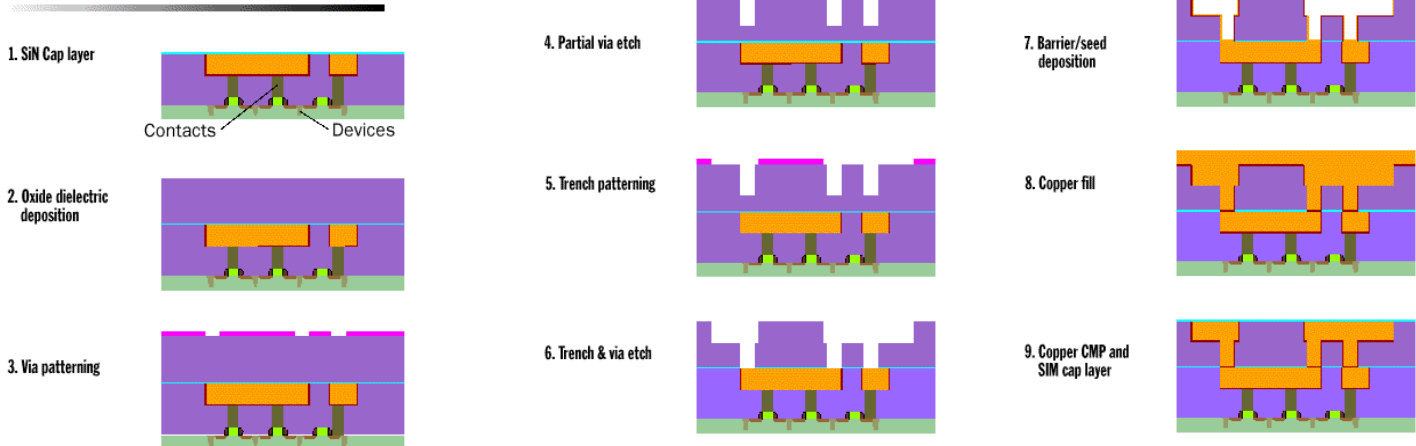
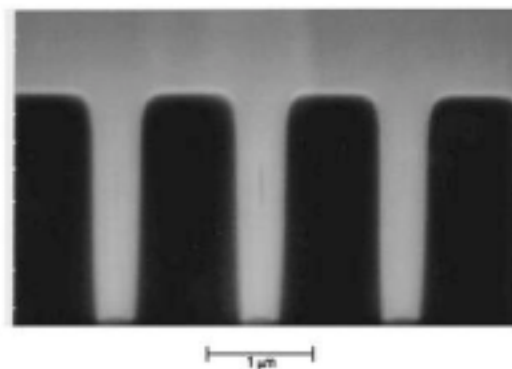
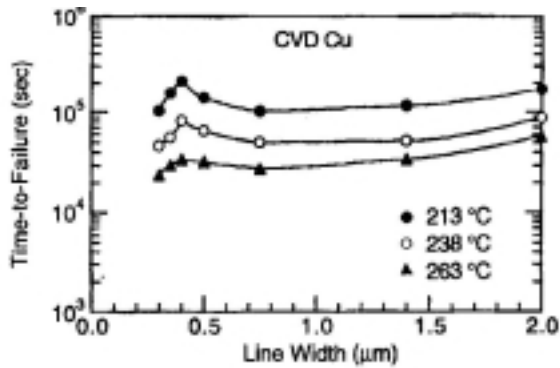


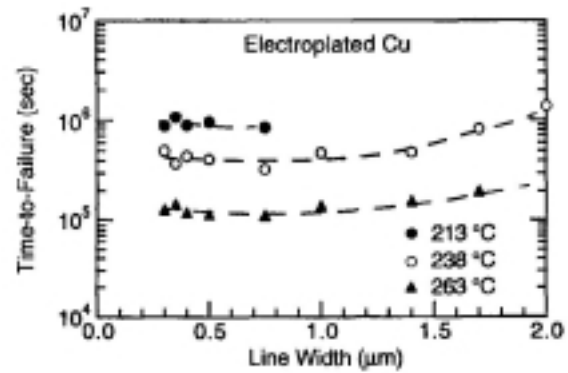
Figure 8. Dual-damascene process flow for fabrication of copper interconnects (From reference 13)

Figure 9. SEM cross-section of high-aspect-ratio trenches (0.28-μm wide, 5.0 aspect ratio) filled by electroplating. These trenches were plated over a tantalum barrier layer and a copper seed-layer, both deposited by PVD (From reference 13).



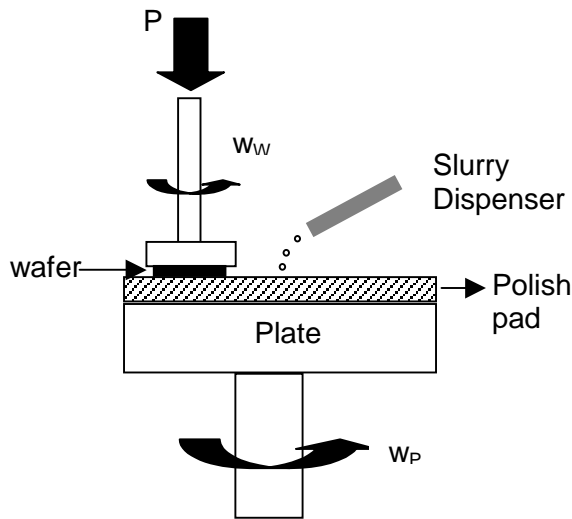


(a)



(b)

Figure 10. Electromigration time-to-failure versus line width of damascene interconnect, a) CVD Cu, b) Electroplated Cu (current density=8 MA/cm²)



CHEMICAL MECHANICAL POLISHING

W_w , W_p : Rotational velocities of wafer holder and the polish plate (15-75 rpm, typically 60 rpm)

P : Pressure applied to wafer (10-50 kPa, typically 30 kPa)

Slurry: Abrasive particles (50-1000 nm sized SiO_2 , Al_2O_3 , CeO_2 or diamond particles with a weight % of 2-7) plus the active chemical ingredients)

Slurry Flow Rate: 20-500 ml/min, typically 200 ml/min.

Figure 11. General features of CMP process (on the right side of the figure some typical numbers pertaining to general CMP process are summarized).

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