

**MSE 125 Term Paper**

**(Ba, Sr)TiO<sub>3</sub> for Multi-Gigabit DRAM**

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## 1. Introduction

Semiconductor memory includes dynamics random access memory (DRAM), static random access memory (SRAM), and non volatile memory(NVM) such as erasable-programmable read only memory(EPROM), electrically erasable ROM(EEPROM), and flash EEPROM. The DRAM type includes frame buffer, fast page-mode(FP) DRAM, Extended Data Output(EDO) DRAM, Synchronous DRAM and Rambus DRAM on the current market.

DRAM is the product that has driven the state of the art of silicon device technology up to the present day. The one-device DRAM cell was invented by R. Dennard at IBM. It consisted of a cell transistor with the drain connected to one node of the cell storage capacitor, the source connected to a bit line, and the gate connected to the word line, which ran orthogonal to the bit line (Figure 1). The requirement to have a large capacitor in a small space with low leakage is the main driving force of DRAM technology.

The criteria for cell choice are density, process simplicity, adequate storage capacitance for detectable signal, and low parasitic capacitance for performance and minimization of noise. DRAM cell size has decreased from 11.3  $\mu\text{m}^2$  for the first 4Mb cell to 0.4  $\mu\text{m}^2$  for the 1Gb cell. Each generation of DRAM must compete with prior generations by providing an ultimate lower cost per bit. This is accomplished by decreasing cell size with each generation, while minimizing the increase in processing cost. The industry trend is to reduce cell size by a factor of 0.33 for each generation. The industry trend in lithography is to reduce the minimum image size by a factor of 0.67 for each generation, so the use of lithography alone would reduce the cell area by 50% for each generation. Therefore technological innovation, involving a change in cell structure, is needed in addition to lithographic scaling to reduce the cell size by a multiple of one third for each generation.

The cell capacitor was a simple planar structure through the 1Mb generation. At and beyond the 4Mb generation, as the cell size decreased, the effective surface area of the capacitor was maintained by placing the capacitor on the sides of a narrow trench etched into the silicon, or by putting the capacitor on top of the other elements of the cell. Figure 2 shows different types of DRAM cell structures. A trench cell is good for small package, it maintains planarity and extends its scalability. However A trench cell is susceptible to noise form the substrate. On the other hand, stack cell becomes the main stream of today's DRAM technology due to its simplicity of fabrication. The rugged surface topology of current nonplanar stack makes it difficult to scale down for future application.

With the increase in the integration of DRAMs, a large charge storage density has been a

requirement for the capacitor. The capacitance ( $C=\epsilon A/t$ ) can be increased by increasing surface area, decreasing dielectric thickness or using insulator materials that have high dielectric constants. Trench cell and stack cell are three dimensional cells which have a large surface area. Additional surface area can be made available by constructing sophisticated cell structure such as fin structure or using porous polysilicon. However the related process technologies are complicated and cost and reliability become issues.  $\text{SiO}_2$  has been used as a standard dielectric in the capacitor due to the process simplicity. The capacitance can be increased by decreasing the thickness of dielectric layer. However it has its practical limit when  $\text{SiO}_2$  thickness reaches direct tunneling region. Defect and breakdown are problems associated with the thin layer  $\text{SiO}_2$ .

Many kinds of dielectric thin films with high relative dielectric permittivities have been actively studied for DRAM capacitor applications, including  $\text{SrTiO}_3$ (ST), La-doped  $\text{PbTiO}_3$  (PLT), and  $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$  (BST). A DRAM capacitor film needs a high dielectric constant, low leakage current and reliability for voltage stress. A method was proposed to evaluate the performance of capacitors by determining charge holding time, the stored charge per unit area[1]. Results are shown in figure 3. It shows that BZT exhibits better performance than silicon nitride with a high dielectric constant and small leakage current. BST is the most promising material because it is a good insulator with large values of relative dielectric permittivity and small values of the dielectric loss near ambient temperature. Its Curies temperature ( $T_c$ ) can be suitable controlled (between  $-162$  to  $120$  °C) by adjusting the ratio of Ba to Sr.

## 2. Deposition methods of (Ba, Sr)TiO<sub>3</sub> thin film

Various deposition methods have been applied to fabricate (Ba, Sr)TiO<sub>3</sub> thin film, including RF-sputtering[2-3], multi-ion beam reactive sputtering[4], pulsed laser deposition[5], metal-organic chemical vapor deposition[6], sol-gel processing[7] and hydrothermal-electrochemical method[8]. ECR sputtering is one of the commonly used deposition method of (Ba, Sr)TiO<sub>3</sub> thin film where O<sub>2</sub> is excited by ECR and substrate temperature can be reduced to 400-700°C.

Sputtering deposition can be divided into four categories: DC, RF, magnetron, and reactive. RF sputtering uses 13.56MHZ frequency, the electrons oscillating in the glow region acquire enough energy to cause ionization collision. RF voltage can be coupled through impedance so that insulating thin film can be deposited. The target self-biases to a negative potential due to the mobility of electrons. More voltage is dropped across the capacitor of a smaller surface area. In magnetron sputtering, electrons in the magnetic field environment experience Lorentz force and move in helical motion, their residence time in the plasma is prolonged and the probability of ion collision is enhanced. This leads to larger discharge currents and increased sputter deposition rates. Electrons are also trapped by Lorentz force near the target, and the ionization efficiency is enhanced there.

Microwave based electron cyclotron resonance (ECR) plasma are electrodeless plasma. Microwave energy is coupled to the nature resonant frequency of the plasma electrons in the presence of a static magnetic field. The condition for energy absorption is that the microwave frequency (commonly 2.45GHZ)  $\omega=qB/m$ , where B is the magnetic field and equals to 0.875

Tesla for required frequency. An ECR device is shown in figure 4. The device consists of a source region, which typically two large electromagnetic coils outside the chamber. The microwaves enter the chamber through a port at the top. The gas is introduced into the source through a leak valve. The substrate is located outside of the plasma chamber. The degree of ionization of ECR plasma is about 1000 times higher than that of RF plasma. One significant benefit of microwave plasma processing is the ability to produce high quality films at a low substrate temperature with minimized contamination.

$Ba_xSr_{1-x}TiO_3$  was chosen to apply to a practical stacked DRAM as a high dielectric constant material [2]. The capacitor fabrication process flow is shown in figure 5. After the storage node contact was opened by dry etching technique, it was filled with the in-situ doped poly Si and etched back. After 50nm thick Ta and 50nm thick Pt films were sputtered at room temperature, the double-layer material was patterned to the node electrode shape by dry etching using HBr gas. The  $(Ba_{0.5}Sr_{0.5})TiO_3$  film was deposited at 650°C in the thickness range of 70-200nm by RF-magnetron sputtering. After 100nm thick CVD- $SiO_2$  film was deposited, it was etched back to leave a  $SiO_2$  sidewall at the node electrode. This structure reduced the leakage current due to poor step coverage of the sputter deposited  $(Ba_{0.5}Sr_{0.5})TiO_3$  film. Finally a 100nm thick TiN film was sputtered as a top electrode. Figure 6 shows the dependence of dielectric constant on film thickness. The dielectric constant was measured at a frequency of 10kHz. The dielectric constant decreased as the film thickness decreased. The dielectric constant of the 70nm thick film was more than 300, which was much larger than that of  $SrTiO_3$ . It was equivalent to a  $SiO_2$  thickness of 8 Å.

A planar stacked capacitor 256Mbit DRAM cell was also developed with a thin film  $(Ba_{0.75}Sr_{0.25})TiO_3$  which had sufficient equivalent  $SiO_2$  thickness of 0.47nm and small leakage characteristics of less than  $1 \times 10^{-7} A/cm^2$ [3]. BST thin film was deposited by a RF-sputtering method using the  $(Ba_{0.75}Sr_{0.25})TiO_3$  ceramic target. In the sputtering process, the substrate temperature was specially cared for the film crystallinity, the dielectric constant and the leakage current characteristics. Figure 7 is the schematic cross section of a 256Mbit DRAM cell. Thin film of  $(Ba_{0.75}Sr_{0.25})TiO_3$  was developed for the capacitor dielectric film and platinum electrodes were adopted for both storage node and cell plate.

Multi-ion-beam reactive sputtering technique (MIBERS) has been successfully applied to the growth of barium strontium titanate  $(Ba_xSr_{1-x})TiO_3$  (BST) thin film[4]. The main features of the MIBERS are independent, adjustable ion beam energy and flux and controllable bombardment by secondary low energy ion source to assist thin film growth. This technique was demonstrated to have very uniform thickness and composition over large area and good process reproducibility. Three focused  $Ar^+$  beams were used to sputter a SrO, BaO and a Ti metal target, respectively. The chamber was first pumped down to a base pressure of  $2 \times 10^{-6}$  Torr by cryopump. Then the argon was bled through the ion guns and oxygen was bled into the chamber directly (molecular ratio of  $Ar/O_2$  was 1), giving rise to a total pressure of about  $4 \times 10^{-4}$  Torr. The  $(Ba_xSr_{1-x})TiO_3$  (BST) thin films were deposited onto unheated or heated Pt-coated Si substrates.

An intrinsic advantage of pulsed laser deposition (PLD) for the synthesis of multicomponent oxide thin film is its ability to transfer the target stoichiometry to the film because the process is

far from equilibrium. The pulsed laser deposition is suitable for rapid exploration of new complex materials and it has a high deposition rate. There have been investigations on the development of  $(\text{Ba}_{0.75}\text{Sr}_{0.25})\text{TiO}_3$  thin film on (100) MgO single crystal substrates by pulsed laser deposition[5]. The films were deposited using a KrF pulsed excimer laser (248nm) operating at 50Hz and an energy of  $0.8\text{J}/\text{cm}^2$ . Deposition involved focusing the laser onto the target. The interaction of the pulsed laser beam with the target produced a plume of the ablated material that was transported toward the heated substrate placed directly in the line of the plume.

Sol-gel process was also applied to the fabrication of BST thin film because of its simplicity, low processing temperature and the ability of easy composition control in thin films with high quality and microchemical homogeneity[7]. The flow diagram of the sol-gel synthesis of BST is outlined in figure 8. Multicomponent  $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$  ( $x=0.6$ ) sols were synthesized using barium oxide, strontium chloride, and titanium isopropoxide as starting materials. The precursor sol was syringed through  $0.2\ \mu\text{m}$  microfilter onto  $\text{SiO}_2(100\text{nm})/\text{Si}(100\text{nm})$  and  $\text{Pt}(150\text{nm})/\text{Ti}(100\text{nm})/\text{SiO}_2(100\text{nm})/\text{Si}$  substrates. Each layer after a spin coating at 2000rpm for 30 seconds was dried at  $100^\circ\text{C}$ , and baked at  $150^\circ\text{C}$  and then  $250^\circ\text{C}$  on a hot plate for 5 minutes to remove residual organic. The deposition/annealing procedure was repeated several times until a desired thickness was obtained. The perovskit phase was formed by a heat treatment of  $650\text{-}750^\circ\text{C}$  for 2 hours in air atmosphere. The sol-gel derived BST thin film heat treated at  $750^\circ\text{C}$  revealed a crack free uniform microstructure composed of ultrafine grains of approximately 40nm in size, and the BST thin film fabricated on  $\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$  substrate exhibited the relative dielectric permittivity of 310.

The hydrothermal-electrochemical method is also an attractive technique for formation of perovskit-type thin films. This method has the advantage of permitting a perovskit type compound,  $(\text{Ba}, \text{Sr})\text{TiO}_3$ , to be synthesized on an electrode of Ti metal that is electrolyzed anodically in an alkaline solution containing (Ba, Sr) elements at relatively low temperatures ( $100\text{-}200^\circ\text{C}$ ). The electrolytic cell is shown schematically in figure 9. The thickness determining factor in this method was the total current passed through the Ti electrode, and the thickness could be controlled by a factor of several micrometers. Ba/Sr composition could be controlled in aqueous solution of  $(\text{Ba}, \text{Sr})(\text{OH})_2$  by the hydrothermal-electrochemical method.

### **3. Structure and properties of $(\text{Ba}, \text{Sr})\text{TiO}_3$ thin film**

Substrate temperature is an important control parameter for sputtering deposition processes. For thin films deposited at room temperature, the as grown films are essentially amorphous in structure, and a postdeposition annealing (typically  $500\text{-}700^\circ\text{C}$ ) is needed to induce crystallization. X-ray diffraction studies indicate that at higher the annealing temperature, the crystallinity is better, and the dielectric constant is higher. The peaks of  $\text{SrTiO}_3$  are much sharper and higher, which indicates much better crystallinity than that of  $\text{BaTiO}_3$ .

For thin films grow at high temperature, the high substrate temperature provides higher adatom mobility, the films crystallize at about  $400^\circ\text{C}$ . Below  $400^\circ\text{C}$ , the adatom mobility may not have been high enough to induce crystallization. While at a substrate temperature of  $500^\circ\text{C}$ , higher adatom mobility induces preferred orientation (001) in the films. The postdeposition annealing

has no significant effect on well-crystallized films. However, it helps in increasing the grain size, modifying the morphology, and oxidizing the films.

For as-grown films deposited at low substrate temperatures, the microstructure is generally a columnar structure, postdeposition annealing may change the microstructure of as-deposited films due to thermally induced diffusion, nucleation, and growth, depending on the original structures. For amorphous as grown films, the inhomogeneous nucleation and subsequent grain growth may lead to the breakdown of columnar structure, resulting in random polycrystallized grains through the film thickness. For well-crystallized films, however, notable recrystallization may not take place and grain growth may lead to the decrease of the number of columnar boundaries.

Figure 10 shows the two types of microstructures of the  $(\text{Ba}_{0.5}\text{Sr}_{0.5})(\text{Ti}_{0.9}\text{Nb}_{0.1})\text{O}_3$  films grown at room temperature and substrate temperature of  $400^\circ\text{C}$ , and subsequently annealed at  $700^\circ\text{C}$  for 8 hours. The film grown at room temperature and annealed at  $700^\circ\text{C}$  showed polycrystalline grains through the film thickness (multi-grain structure), whereas the films deposited at  $400^\circ\text{C}$  (crystallized films) maintained columnar structure even after annealing at  $700^\circ\text{C}$  for 8 hours.

The dielectric constant and dissipation factor measured at 100KHz and 0.01V oscillation level of  $0.4\mu\text{m}$   $(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3$  films deposited at room temperature followed by postdeposition annealing at  $700^\circ\text{C}$  for 2 hours in oxygen for various Sr content (x) are shown in figure 11. For all compositions, the dielectric constants were low (below 200), and only slightly increased as Sr content increased, it can be attributed to the better crystallinity of  $\text{SrTiO}_3$ .

Figure 12 shows the effect of film thickness on the dielectric constants and dissipation factors for  $(\text{Ba}_x\text{Sr}_{1-x})\text{TiO}_3$  films deposited at room temperature and annealed at  $700^\circ\text{C}$  for 2 hours. The dielectric constant increased with film thickness.

The deposition annealing temperature effect on the dielectric constants and dissipation factors is shown in figure 13 for  $1.2\mu\text{m}$   $\text{SrTiO}_3$  films deposited at room temperature. The dielectric constant increased linearly with annealing temperature. The reason is that higher annealing temperature can result in better crystallinity, at higher annealing temperature, the increase in grain size, as well as reduction of the amount of amorphous phase, may be contributed to the higher dielectric constant.

The reasons for the much lower dielectric constants for BST film deposited at room temperature may be as follow: (a) the very fine grain size as well as less crystallinity due to low temperature processing. (b) surface layer effect due to an oxygen adsorption layer on either surface or grain boundaries. (c) for thin films deposited at low temperature, the microstructure of the films are generally of columnar structure containing voids between columns, and subsequently annealing may not eliminate these voids. Such voids with low dielectric constant will tend to lower the overall dielectric constant of the films.

For BST film deposited at higher temperature, due to its high adatom mobility, the factors which

lowering the dielectric constant can be partly eliminated, including incomplete crystallization, oxygen adsorption layer and voids between columns.

Figure 14 shows the dielectric constants and dissipation factors of BST films deposited at 400°C and postdeposition annealing at 700°C for 2 to 8 hours as a function of Sr content. Only after annealing for long times could the dissipation factors be reduced and thus exhibit the real dielectric constants of films without the contribution from DC conduction. The dielectric constant increased from 237 for BaTiO<sub>3</sub> to a maximum of 563 for (Ba<sub>0.5</sub>Sr<sub>0.5</sub>)TiO<sub>3</sub> and decreased again for higher Sr content.

Figure 15 shows the dielectric constant and dissipation factors of BST film deposited at various substrate temperatures and annealed at the same temperature of 700°C for 8 hours. The dielectric constant between films deposited at room temperature and 200°C suggests that the adatom mobility at a substrate temperature of 200°C is high enough to reduce the voids between the columns.

The thickness effect of dielectric constant and dissipation factor is shown in figure 16 for BST film deposited at 400°C and annealed at 700°C for 8 hours. The dielectric constant dropped from 367 for 0.4μ m films to 255 for 0.2μ m films. Thicker films may exhibit stress effect.

## 4. Conclusions

As the density of DRAM enters into the era of Gigabit density, key technology innovations such as innovated cell structure, high dielectric capacitor, advanced lithography, shallow trench isolation, and low resistance contact need to be developed to meet the stringent requirements. The criteria for cell choice are density, process simplicity, and adequate storage capacitance. High dielectric constant materials such as (BaSr)TiO<sub>3</sub> is used to overcome the reduction of capacitor area. They have very high dielectric constant and equivalent to thin SiO<sub>2</sub>, but don't suffer defect and current tunneling problems.

Various deposition methods, including RF-sputtering, multi-ion beam reactive sputtering, pulsed laser deposition, metal-organic chemical vapor deposition, sol-gel processing and hydrothermal-electrochemical method, have been applied to fabricate (Ba, Sr)TiO<sub>3</sub> thin film. ECR sputtering is one of the commonly used deposition method of (Ba, Sr)TiO<sub>3</sub> thin film due to the reduced substrate temperature compared to regular sputtering.

For BST thin film deposited at higher substrate temperature (400°C), due to its high adatom mobility, the factors which lowering the dielectric constant can be eliminated, including incomplete crystallization, oxygen adsorption layer and voids between columns. The dissipation factors can be reduced after annealing at 700°C for 8 hours. The dielectric constant increases as the thickness of the film increases, however mechanical stress might be developed for thick film. Better crystallinity, thick BST film and minimum stress are the key features for high dielectric constant films. Dielectric constant as high as 560 was reported for sputtered BST thin films.

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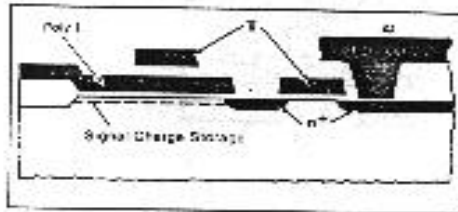


Fig. Flash capacitor cell using two poly gates. The top of cell is used as read electrode. Cells are used in parallel.

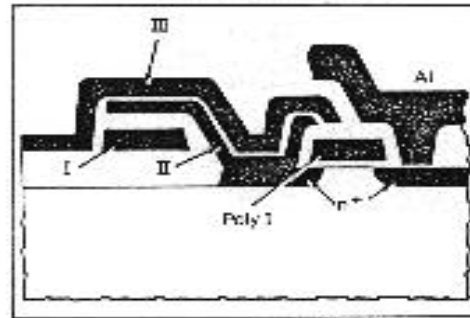


Fig. Stacked capacitor cell (STC) (10), (11). Top capacitor is made between two poly gates I and II and stored over the second transistor.

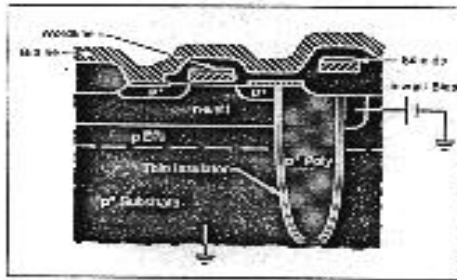


Fig. Substrate-plate flash capacitor cell (12). The concept of using the trench capacitor is to store the signal charge on the poly lines. In the trench used to form the gate stacks, especially the heavily doped substrate, are the capacitive read electrodes. Also, the stress device is made to reduce the cell area and to reduce the cell area.

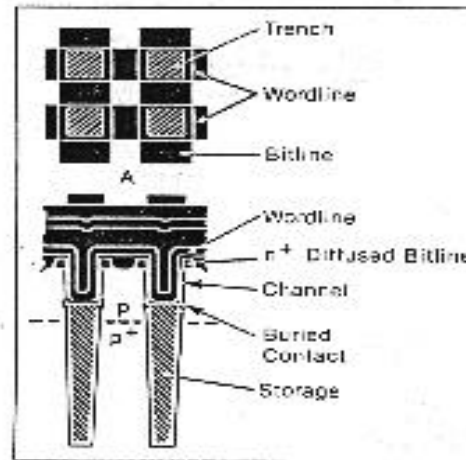


Fig. Transistor cell (13). A cell is a trench capacitor, over the cell cross structure between wordline.

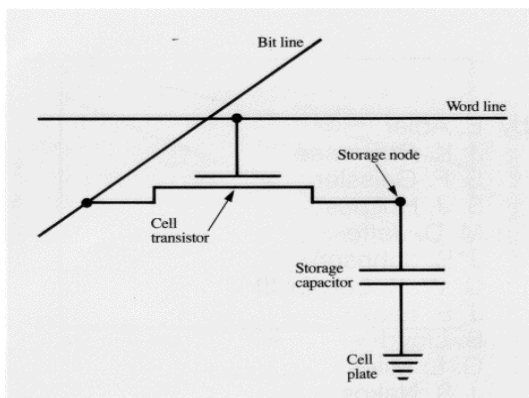


Figure 1

The one-transistor cell, consisting of a storage capacitor and a single transistor through which it is accessed.

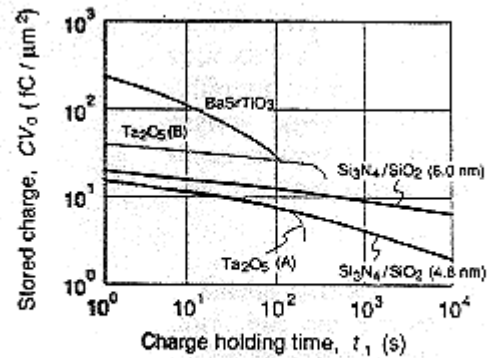


Fig. 3 Stored charge corresponding to the holding time defined by sustaining 90% of the initial charge.

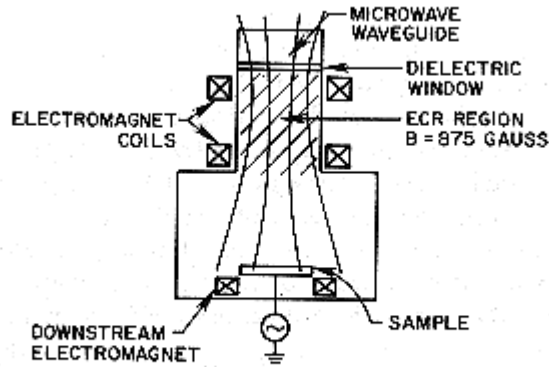


Fig. 4 Electron cyclotron resonance (ECR) plasma device in the axial geometry. The sample position is at the bottom and may be biased.

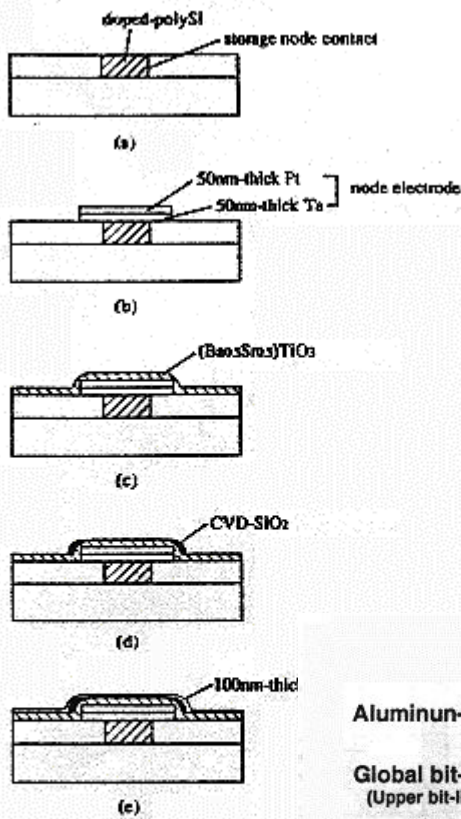


Fig.5 Capacitor fabrication process  
 (a) storage node contact format  
 (b) node electrode patterning  
 (c) (Ba<sub>0.5</sub>Sr<sub>0.5</sub>)TiO<sub>3</sub> sputtering  
 (d) CVD-SiO<sub>2</sub> sidewall format  
 (e) top electrode formation

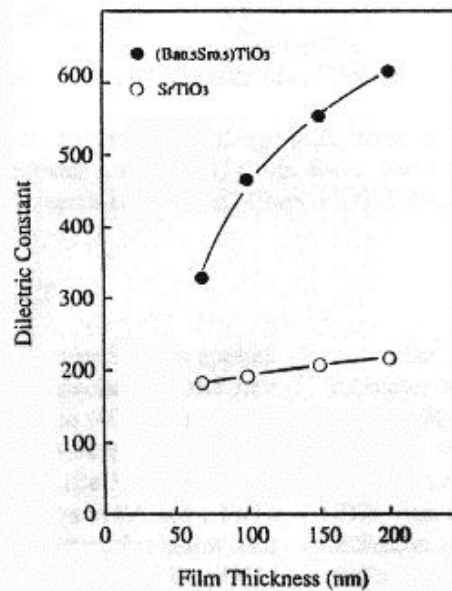


Fig.6 Dependence of dielectric constant on film thickness

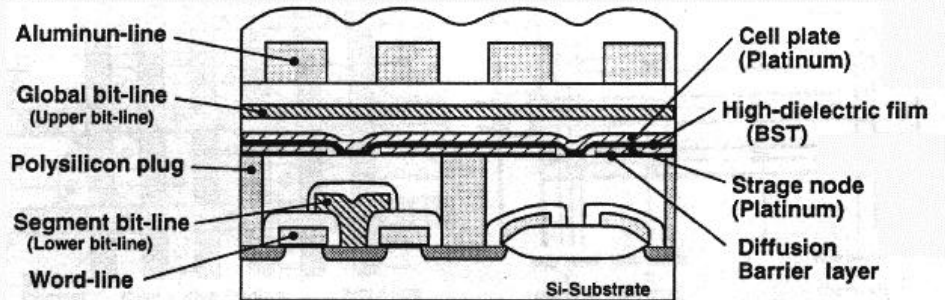


FIG . Schematic cross sectional view of planar stacked capacitor cell with high-dielectric constant film.

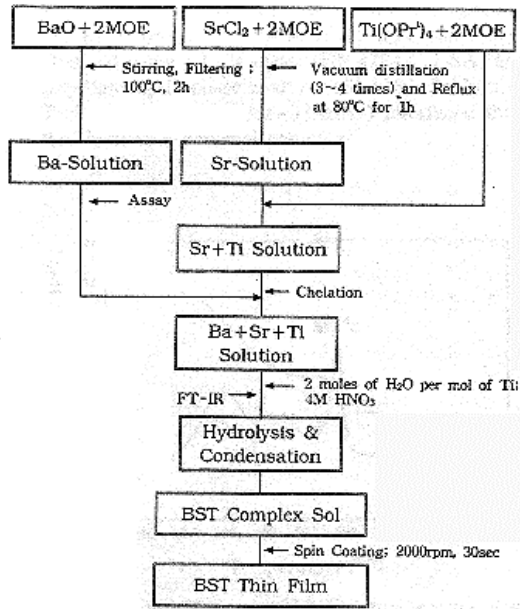


FIG. 8 Flow diagram for the synthesis of BST sol.

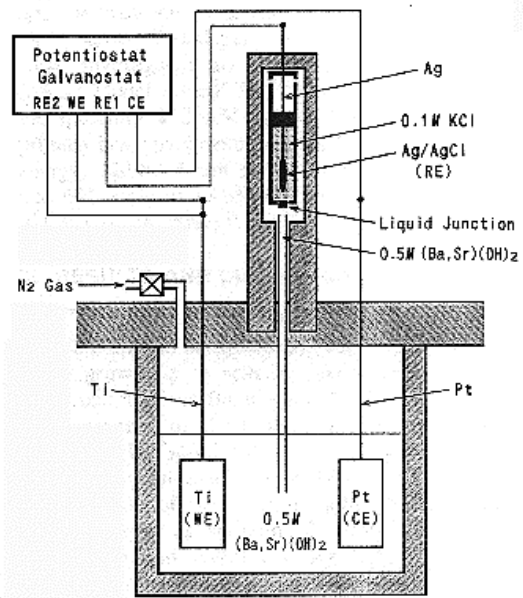


FIG. 9 Electrolytic cell equipped with a Ag/AgCl external reference electrode. Electrolysis was performed potentiostatically by the three-electrode technique.

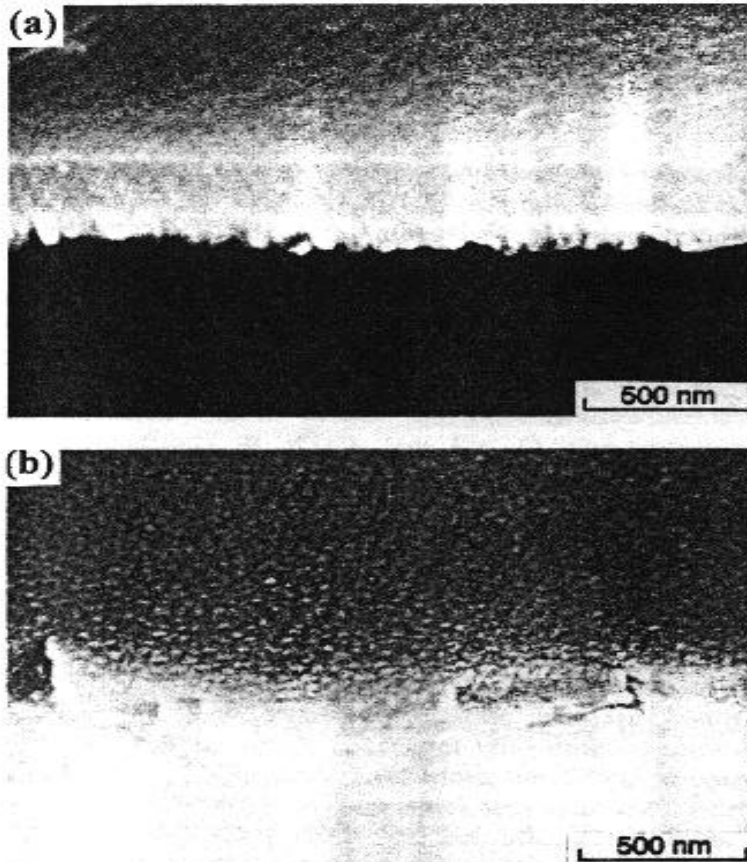


FIG. 10 Surface morphology of  $(\text{Ba}_{0.5}\text{Sr}_{0.5})(\text{Ti}_{0.9}\text{Nb}_{0.1})\text{O}_3$  films grown at (a)  $T_s = 400^\circ\text{C}$  and (b)  $T_s = \text{RT}$  and subsequently annealed at  $700^\circ\text{C}$  for 8 h.

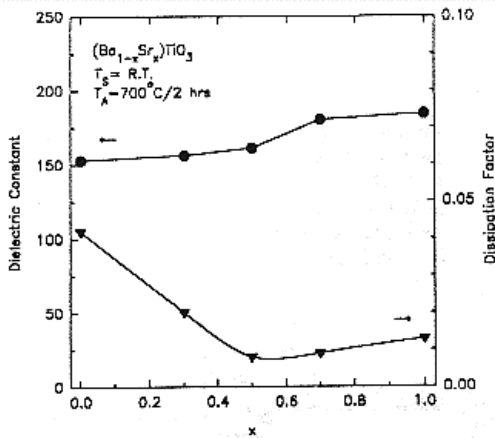


FIG. 11 Dielectric constant and dissipation factor of  $0.4 \mu\text{m}$   $(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$  films deposited at  $T_s = \text{RT}$  and annealed at  $700^\circ\text{C}$  for 2 h for various Sr content  $x$ .

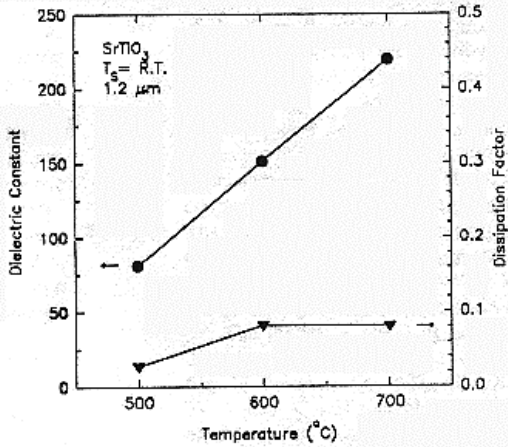


FIG. 13 Dielectric constant and dissipation factor of  $1.2 \mu\text{m}$  for  $\text{SrTiO}_3$  films ( $\text{Sr}/\text{Ti} = 1.03$ ) deposited at  $T_s = \text{RT}$  and annealed at various temperatures for 2 h.

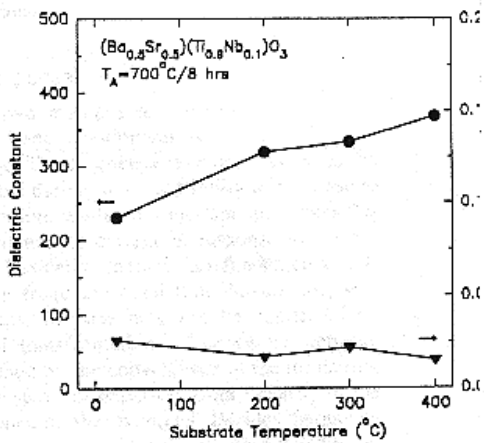


FIG. 15 Dielectric constant and dissipation factor of  $0.4 \mu\text{m}$   $(\text{Ba}_{0.5}\text{Sr}_{0.5})(\text{Ti}_{0.9}\text{Nb}_{0.1})\text{O}_3$  films deposited at various temperatures and subsequently annealed at  $700^\circ\text{C}$  for 8 h.

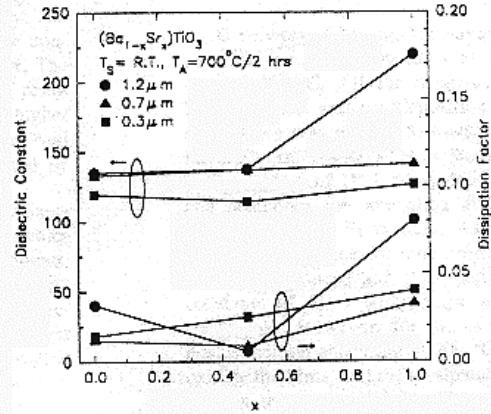


FIG. 12 Dielectric constant and dissipation factor of  $\text{BaTiO}_3$ ,  $\text{SrTiO}_3$  ( $\text{Ba}/\text{Ti}$  and  $\text{Sr}/\text{Ti} = 1.03$ ), and  $(\text{Ba}_{0.5}\text{Sr}_{0.5})\text{TiO}_3$  films grown at  $T_s = \text{RT}$  and annealed at  $700^\circ\text{C}$  for 2 h with various thickness.

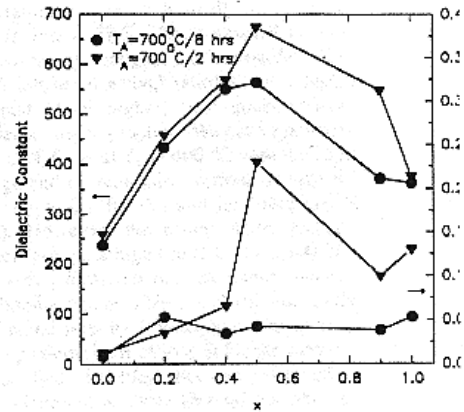


FIG. 14 Dielectric constant and dissipation factor of  $0.4 \mu\text{m}$   $(\text{E}, \text{Sr})\text{TiO}_3$  films deposited at  $T_s = 400^\circ\text{C}$  and annealed at  $700^\circ\text{C}$  for 2 and 8 h with various Sr content  $x$ .

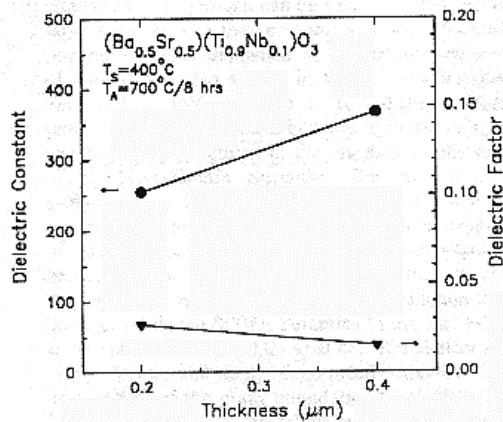


FIG. 16 The thickness effect of *in situ* crystallized films on the dielectric constant and dissipation factor for  $(\text{Ba}_{0.5}\text{Sr}_{0.5})(\text{Ti}_{0.9}\text{Nb}_{0.1})\text{O}_3$  films deposited at  $T_s = 400^\circ\text{C}$  and annealed at  $700^\circ\text{C}$  for 8 h.